

Schematic Package Supplement to

Kangaroo™

Operation, Maintenance and Service Manual

NOTE

This staple temporarily holds the schematic package together. Remove the staple before using the schematics.



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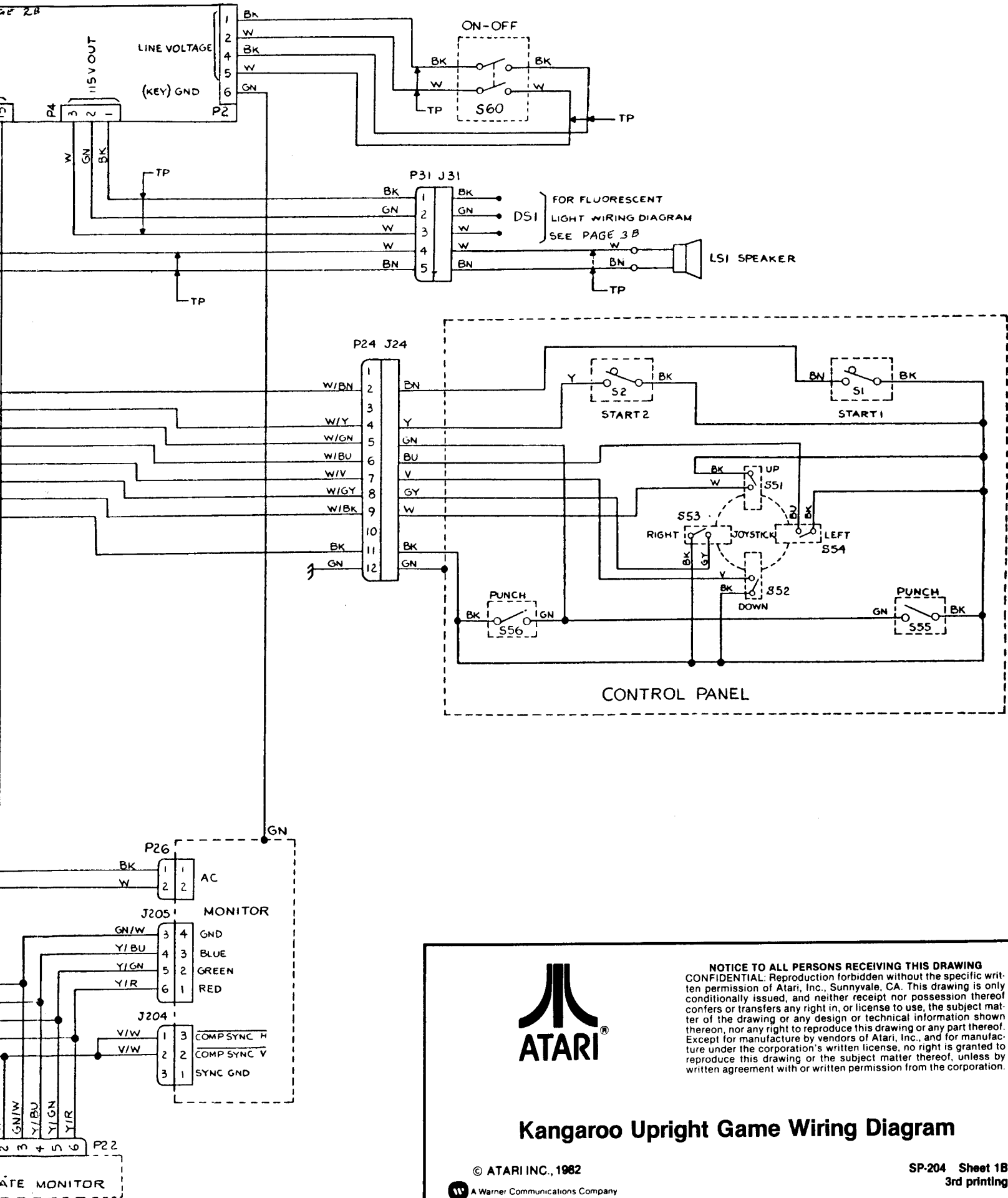
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Kangaroo Upright Game Wiring Diagram

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KANGAROO CPU PCB

- PCN 2
- +5V RTN W
 - SENSE 19 R/IGN
 - +SENSE 21 R/BU
 - +5V REG Y R/Y
 - +12VDC Z R/IGN
 - INVERT D R/W
 - GND 16 R/W
 - SOUND C BK
 - GND 18 BK
 - SPKR RTN T W
 - SPKR OR
 - START 1 A W/BN
 - START 2 I W/Y
 - PUNCH 6 W/IGN
 - LEFT E W/BU
 - DOWN F W/V
 - RIGHT 4 W/GY
 - UP 5 W/BK
 - GND U BK
 - L COIN 8 Y
 - R COIN 2 OR
 - GND 17 BK
 - COIN CNTR L 14 V/BK
 - COIN CNTR R 5 BU/BK
 - TEST J W
 - GND V BK

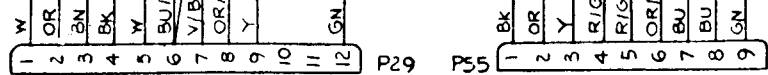
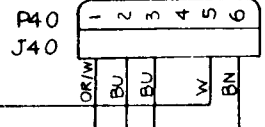
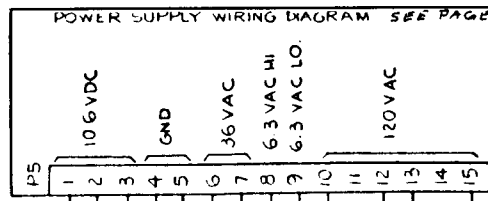
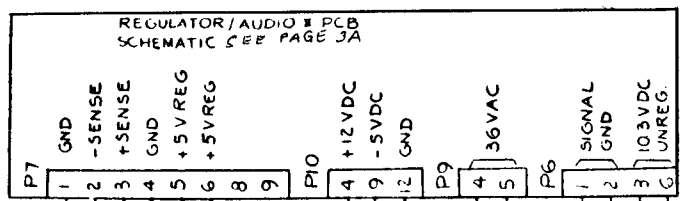


- PCN 1
- +5V RET H R/IGN
 - +5V REG J R/W
 - +12VDC K W/BN
 - 5VDC L R/BK

KANGAROO VIDEO PCB

- VIDEO GND E GN/W
- BLUE C Y/BU
- GREEN B Y/GN
- RED A Y/R
- COMP SYNC D V/W

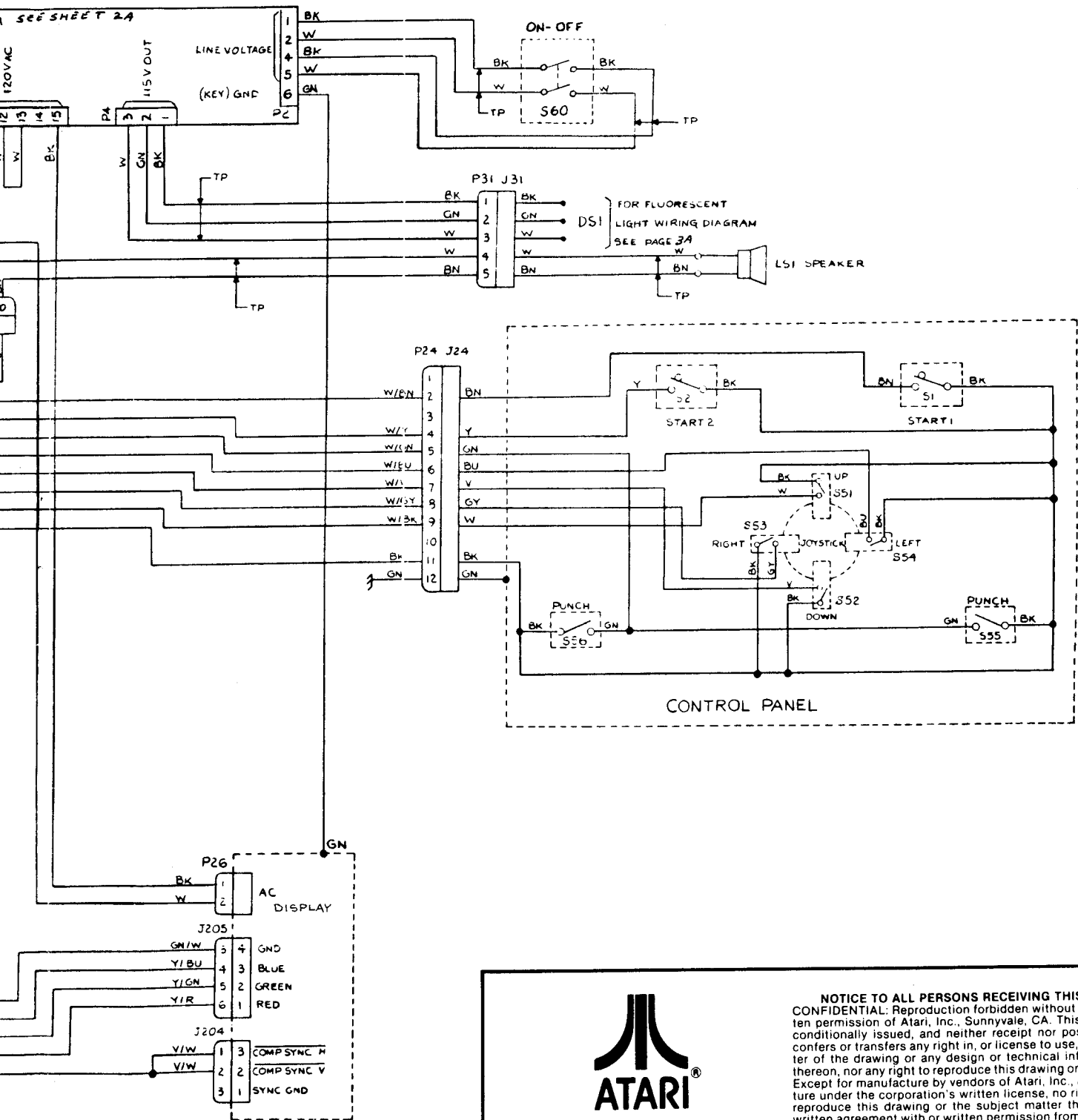
PCN 4:



FOR COMPONENT WIRING DIAGRAM SEE PAGE 3B

FOR COIN DOOR WIRING DIAGRAM SEE PAGE 3B

ALTERNATE



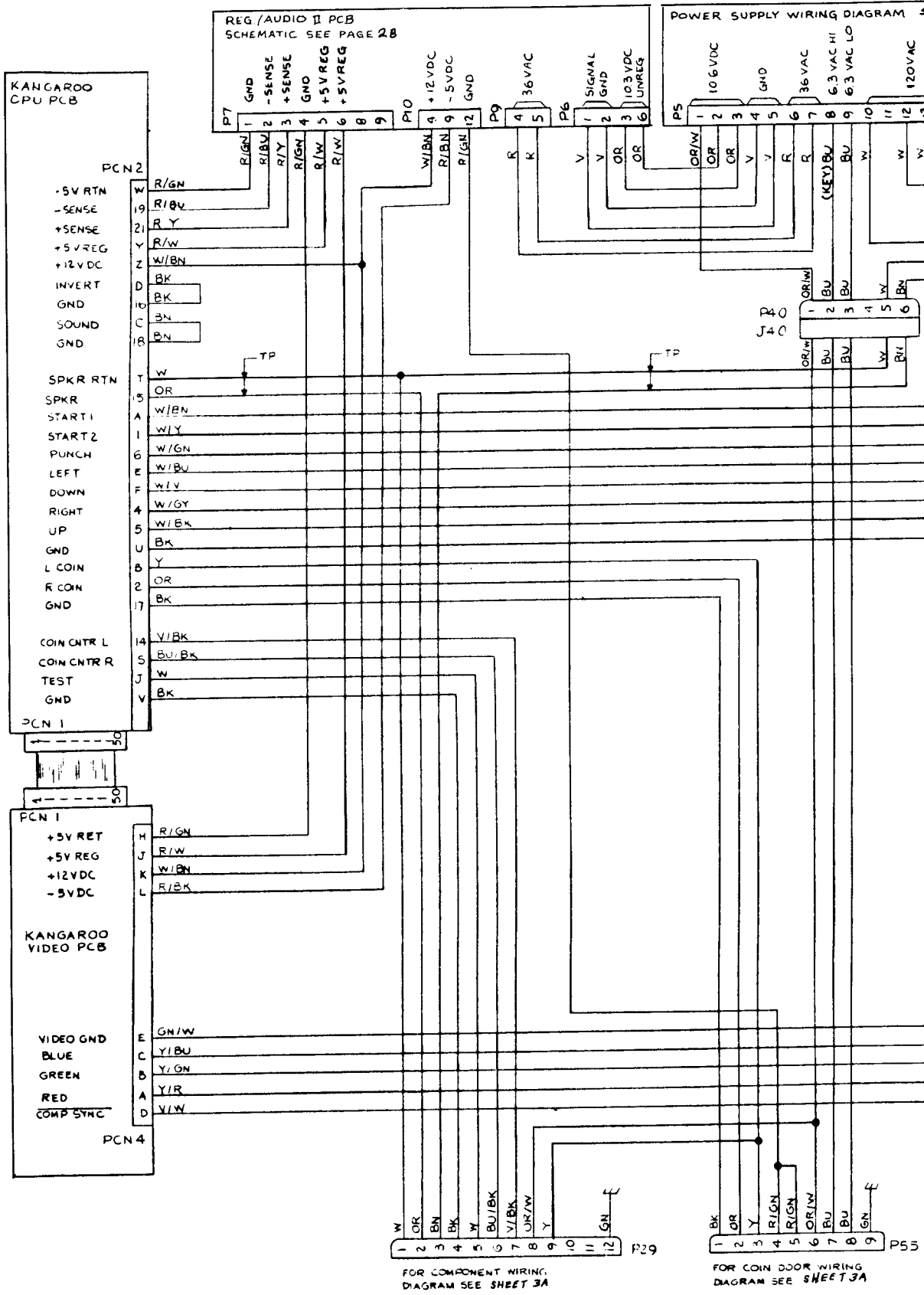
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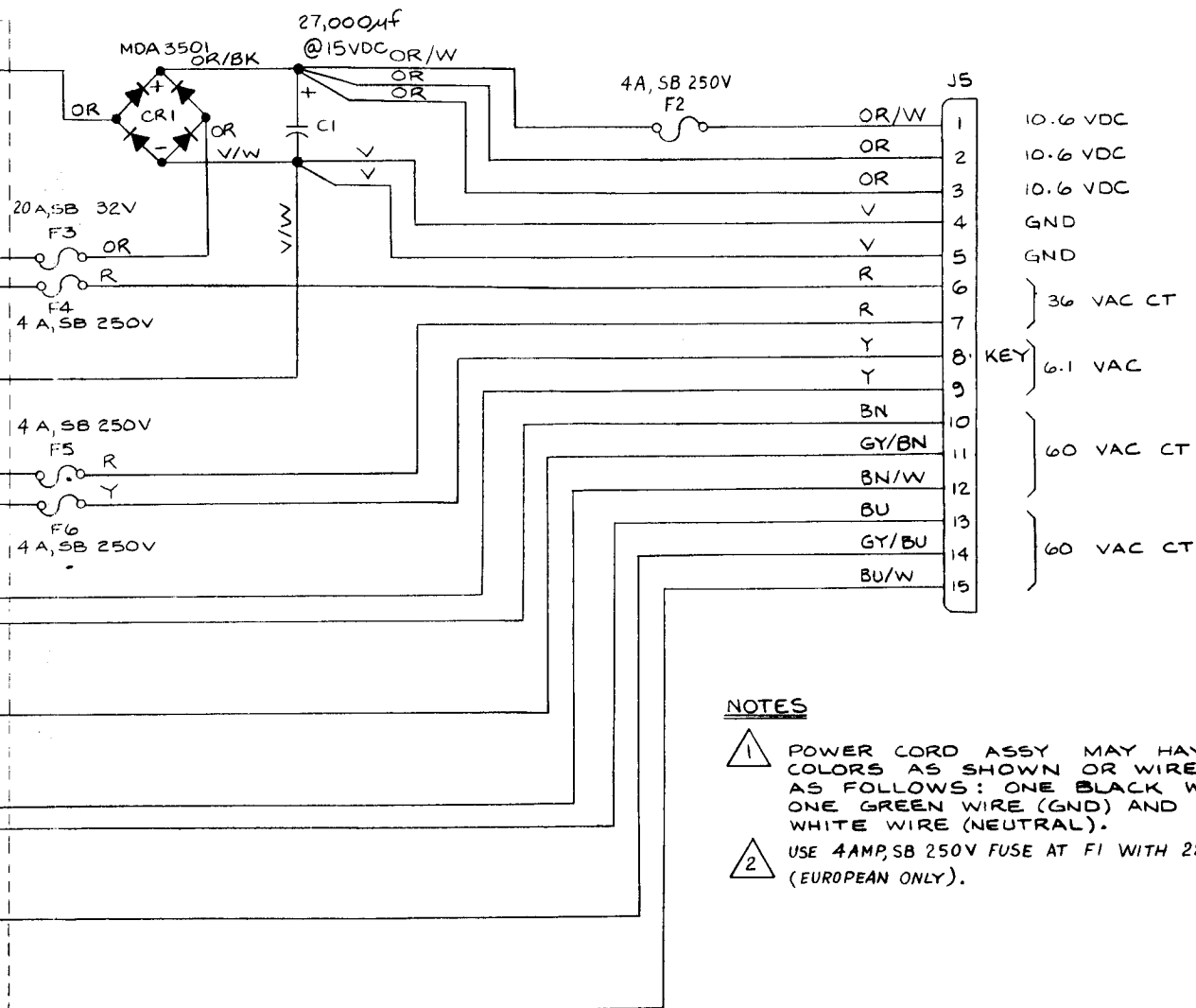
Ireland-Built Kangaroo Game Wiring Diagram

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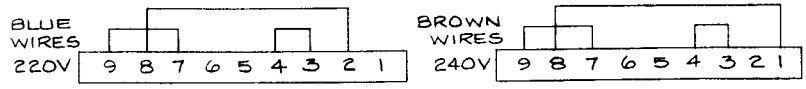
NOTES

- ⚠️ POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
- ⚠️ USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).

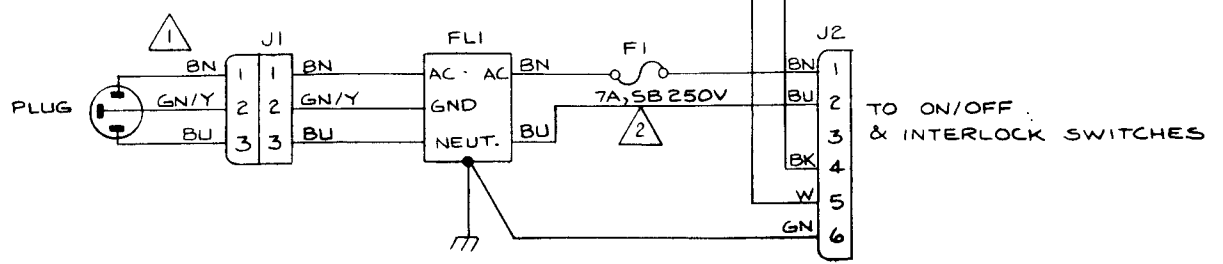
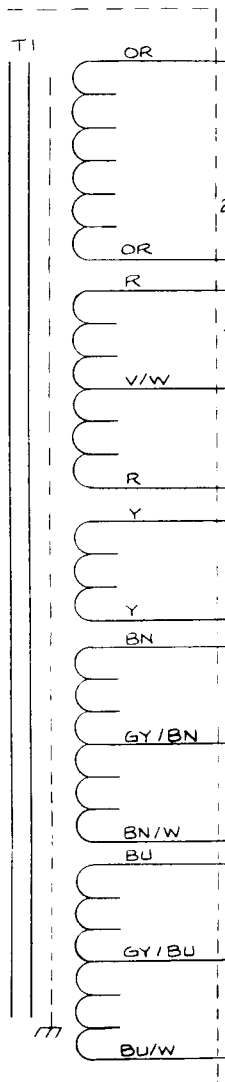
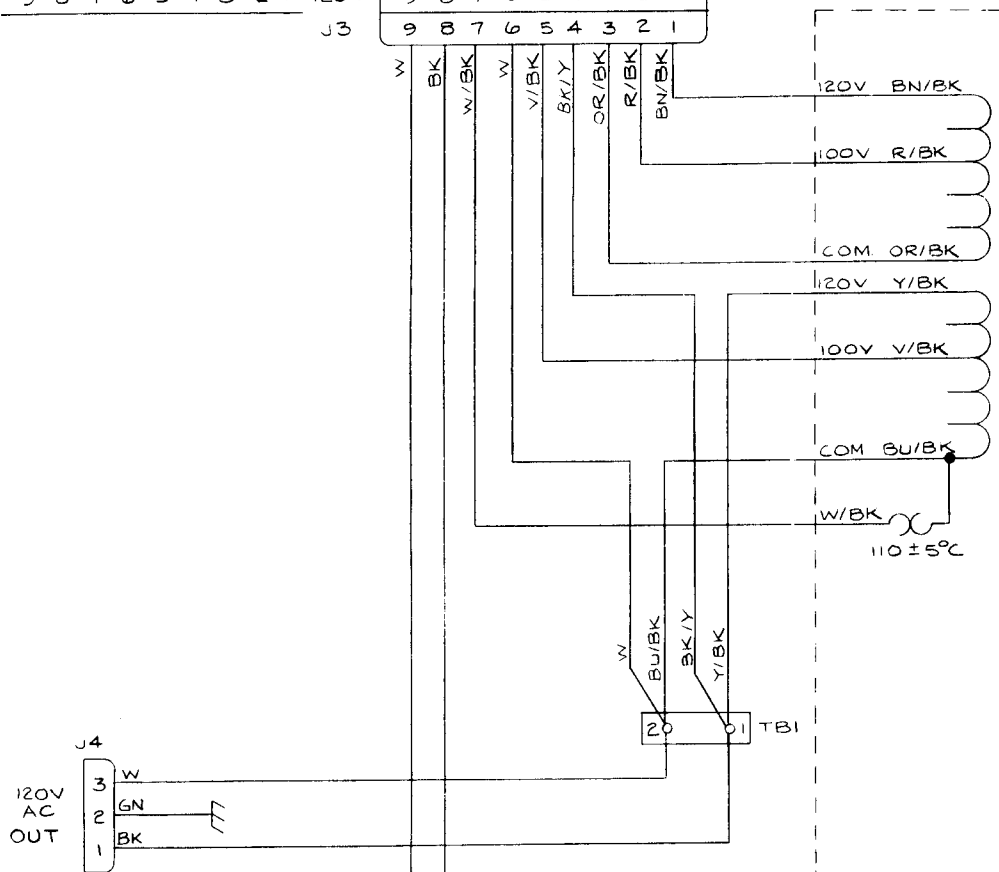
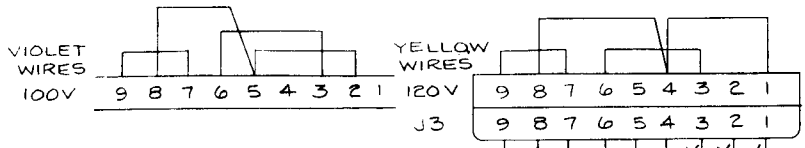


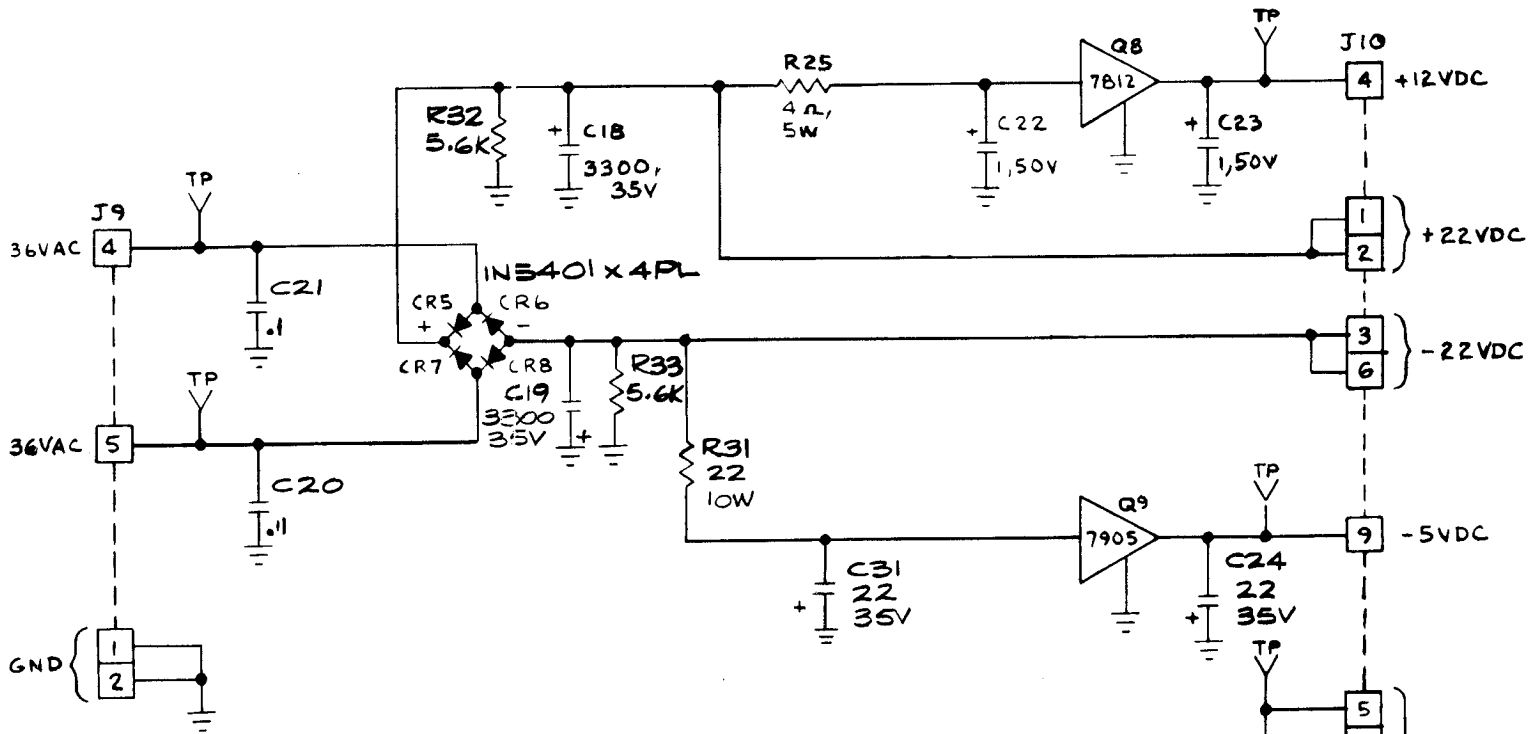
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Kangaroo Power Supply

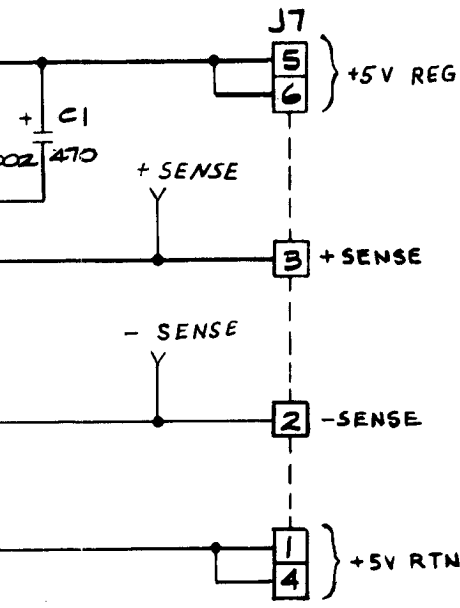


VOLTAGE SELECTION BLOCKS



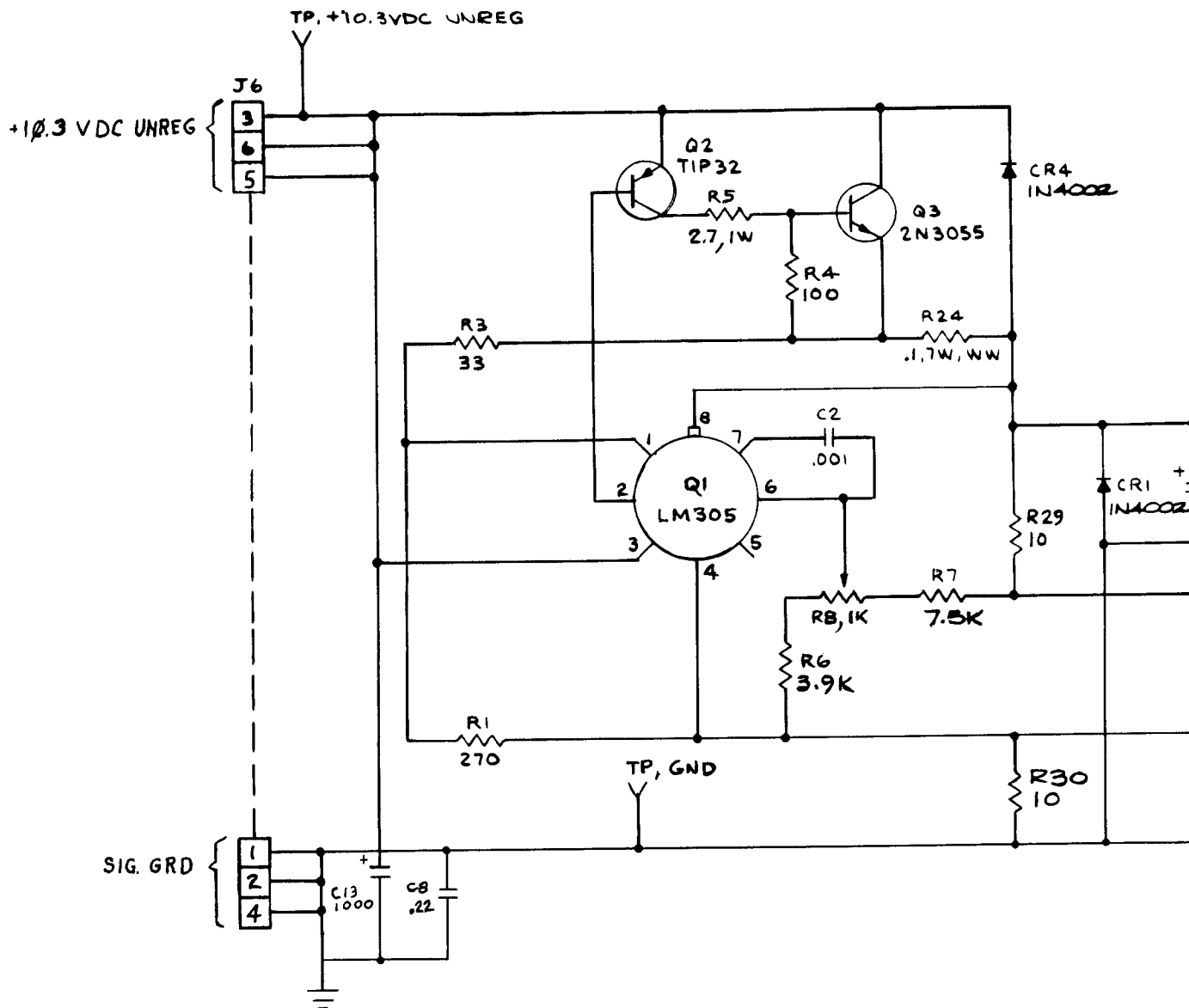


| LAST DES | NOT USED |
|----------|--------------------------|
| C31 | C3-7, 9-12, 14-17, 25-30 |
| CR8 | CR2, 3 |
| Q11 | Q10, 11, 4, 6 |
| R33 | R2, 9-23, 26-28 |

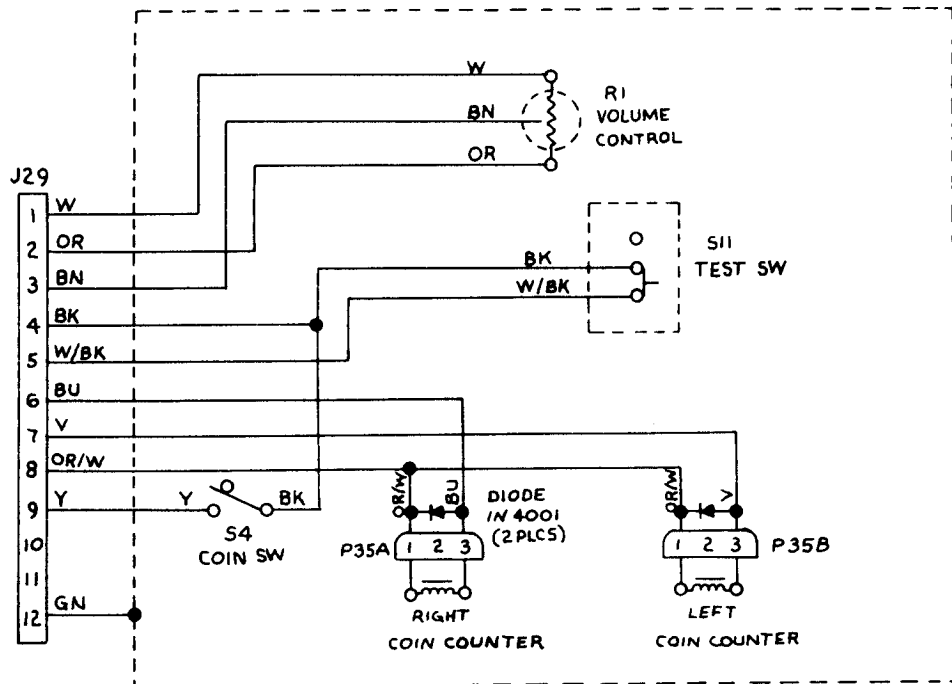


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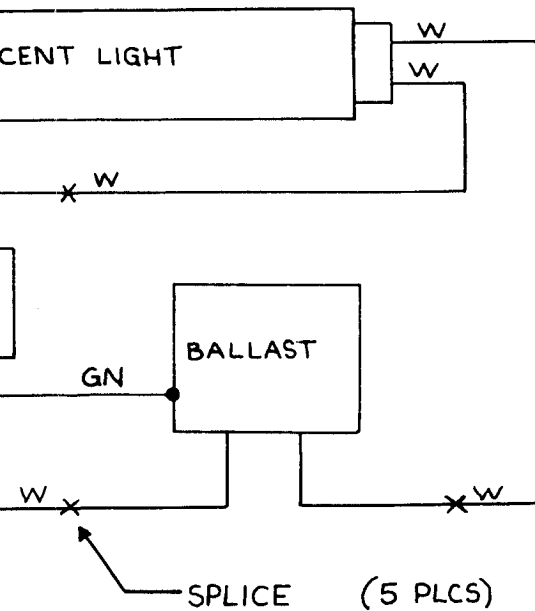
Kangaroo Reg./Audio II PCB Schematic Diagram



Utility Panel Wiring Diagram



Speaker Wiring Diagram



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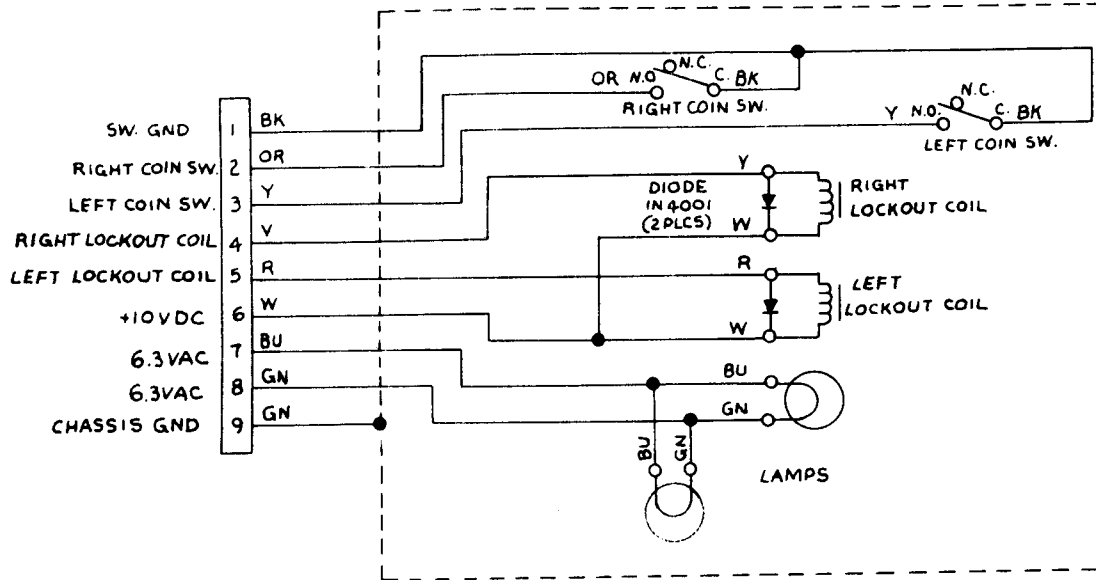
Kangaroo Game Wiring Interfaces

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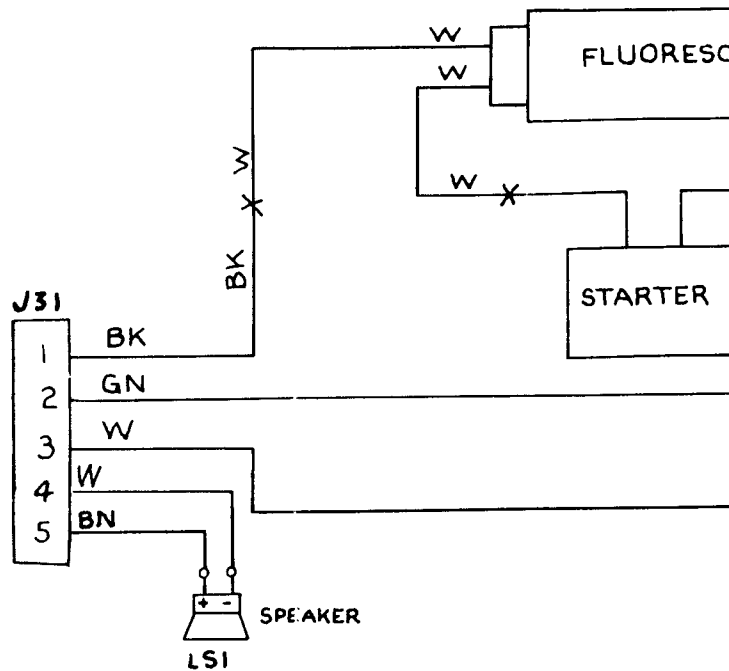
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Coin Door Wiring Diagram

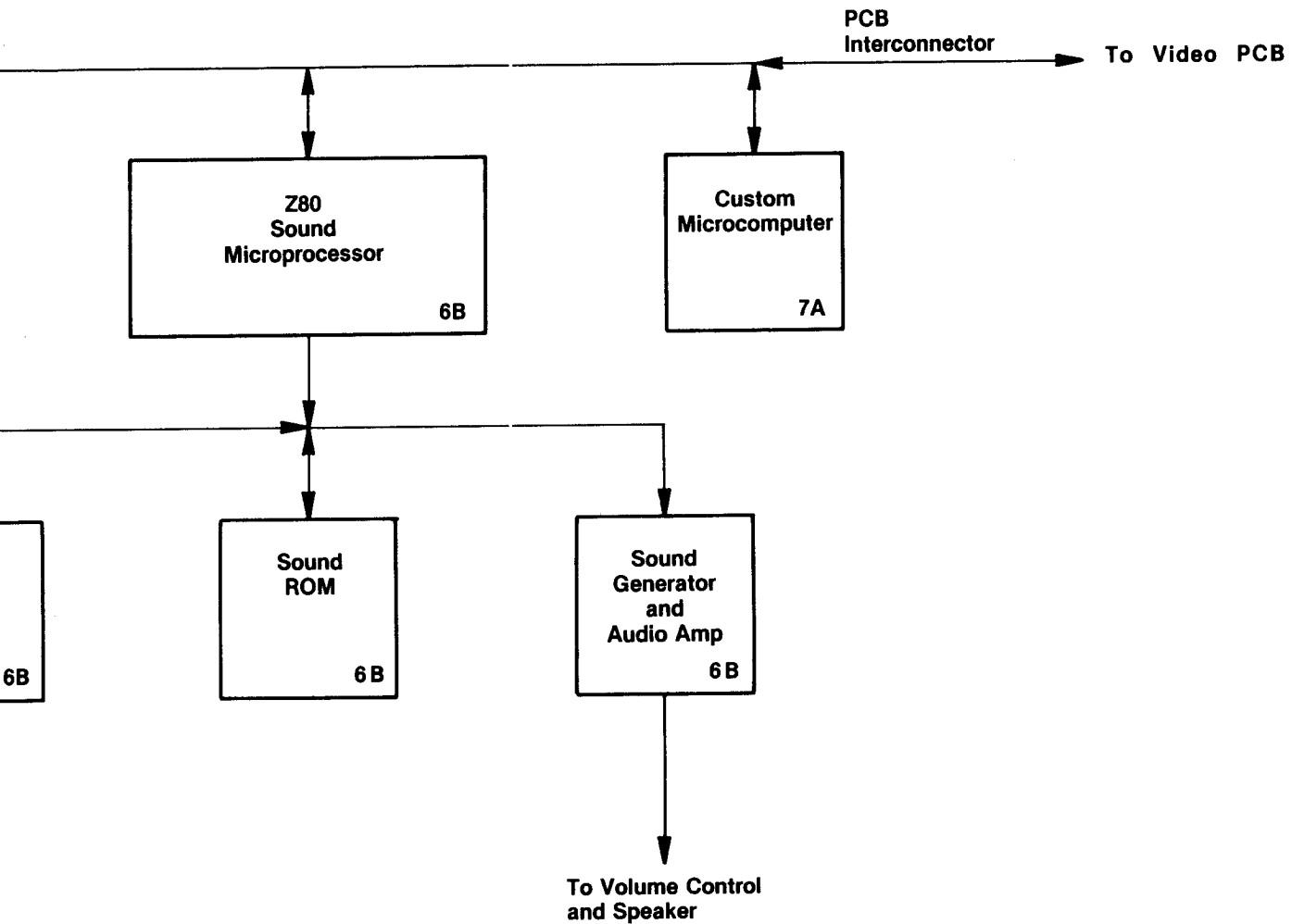


Fluorescent Light and



NOTE

The **service switch**, located on the CPU PCB, allows you to enter credits without tripping the coin counter.



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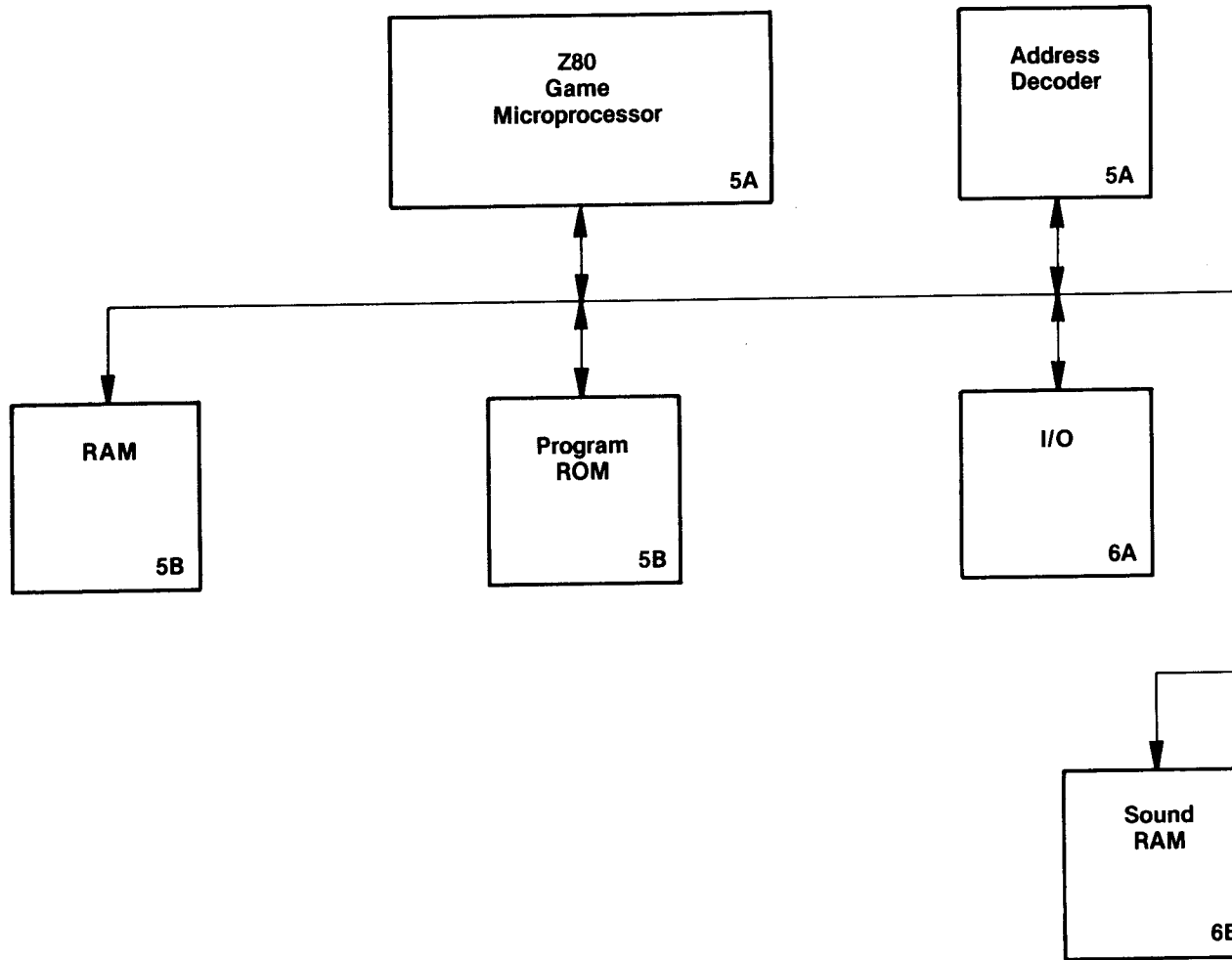
Kangaroo CPU PCB Schematic Diagram

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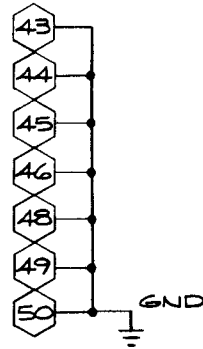
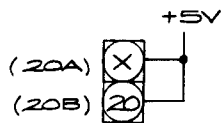
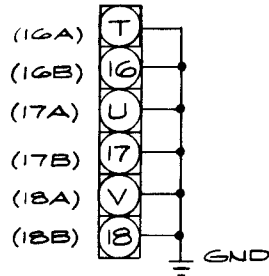
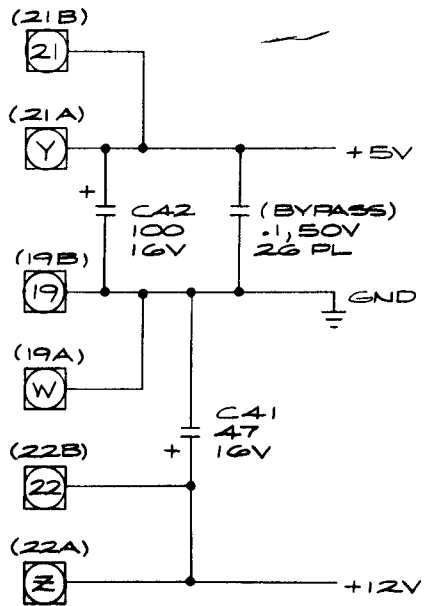
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Block Diagram (CPU PCB)



CPU Power Input



NOTES:

1.  = CONNECTOR CN2
2.  = CONNECTOR CN1



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Kangaroo CPU PCB Schematic Diagram

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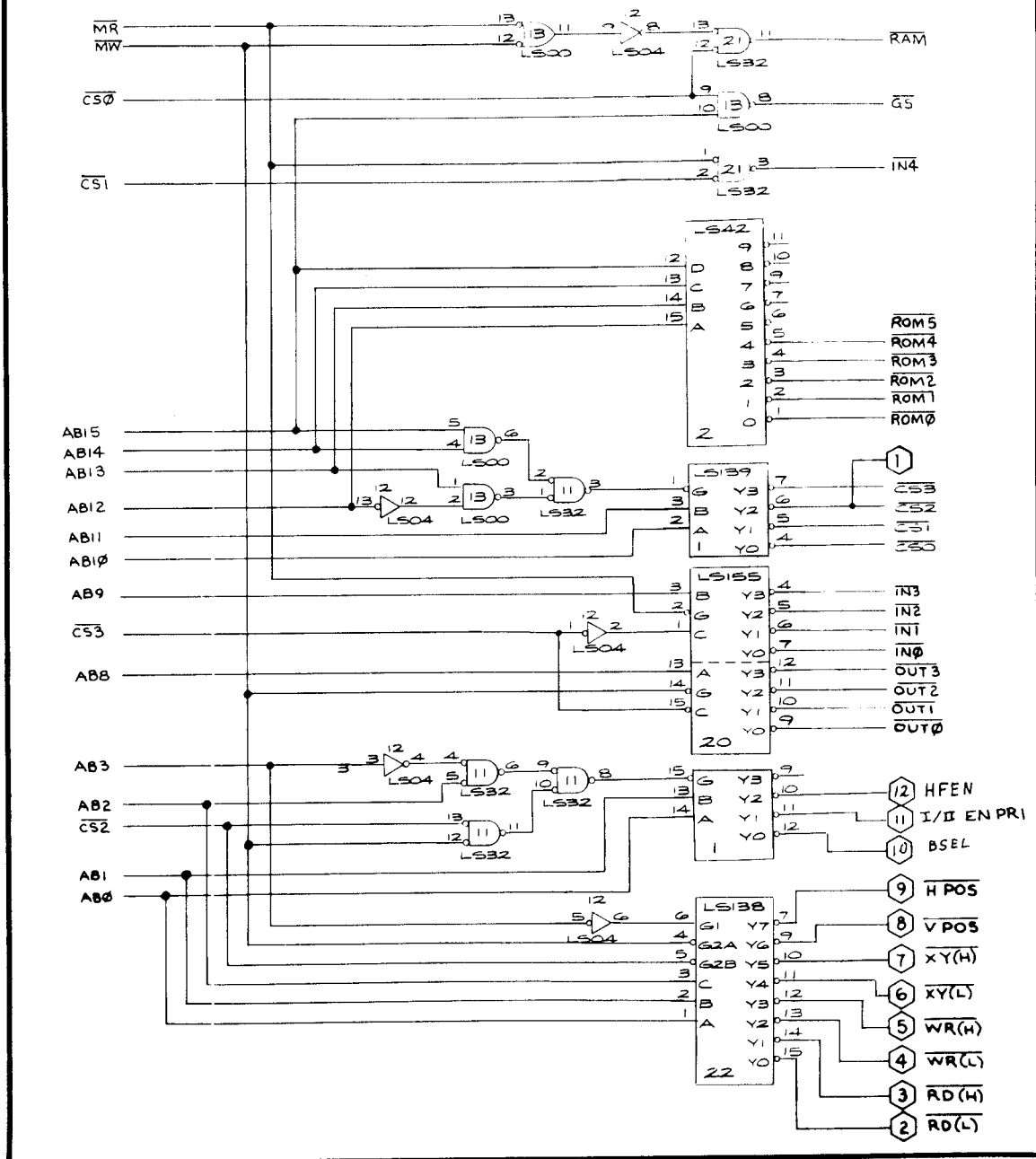
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Memory Map

| HEXA-DECIMAL ADDRESS | R/W | DATA D7 D6 D5 D4 D3 D2 D1 D0 | | | | | | | | FUNCTION |
|---|-----|---------------------------------|---|---|---|---|---|---|---|--|
| Game Microprocessor Memory Space (IC15) | | | | | | | | | | |
| 0000-5FFF | R | D | D | D | D | D | D | D | D | Z80 24K Program ROM |
| E000-E3FF | R/W | D | D | D | D | D | D | D | D | 1K Working RAM |
| E400 | R | D | D | D | D | D | D | D | D | Option Switch |
| E800 | W | D | D | D | D | D | D | D | D | Low Byte } Start Address of Data in Picture High Byte } ROM for DMA |
| E801 | W | D | D | D | D | D | D | D | D | |
| E802 | W | D | D | D | D | D | D | D | D | Low Byte } Start Address in Bit Map RAM (where High Byte } picture is to be written) During DMA |
| E803 | W | D | D | D | D | D | D | D | D | |
| E804 | W | D | D | D | D | D | D | D | D | Low Byte } Picture Size for DMA High Byte } and DMA Start |
| E805 | W | D | D | D | D | D | D | D | D | |
| E806 | W | D | D | D | D | D | D | D | D | Vertical Start Address in Bit Map |
| E807 | W | D | D | D | D | D | D | D | D | Horizontal Start Address in Bit Map |
| E808 | W | | | | | | | D | D | Bank Select Latch |
| E809 | W | | | | D | D | D | D | D | A & B Bit Map Control Latch (A = playfield, B = motion) |
| E80A | | | | | D | D | D | D | D | Color-Shading Latch |
| EC00 | W | D | D | D | D | D | D | D | D | Sound DATA to Sound Microprocessor |
| EC00 | R | | | | | | | | D | Utility Coin Switch |
| EC00 | R | | | | | | | D | | 1 Player Start |
| EC00 | R | | | | | D | | | | 2 Player Start |
| EC00 | R | | | | | D | | | | Left Coin Input |
| EC00 | R | | | | D | | | | | Right Coin Input |
| ED00 | W | | | | | | | | D | Coin Counter 1 |
| ED00 | W | | | | | | | D | | Coin Counter 2 (European games) |
| ED00 | R | | | | | | | | D | Player 1 Right |
| ED00 | R | | | | | | | D | | Player 1 Left |
| ED00 | R | | | | | D | | | | Player 1 Up |
| ED00 | R | | | | D | | | | | Player 1 Down |
| ED00 | R | | | | D | | | | | Player 1 Punch |
| EE00 | R | | | | | | | | D | Player 2 Right |
| EE00 | R | | | | | | | D | | Player 2 Left |
| EE00 | R | | | | | D | | | | Player 2 Up |
| EE00 | R | | | | D | | | | | Player 2 Down |
| EE00 | R | | | | D | | | | | Player 2 Punch |
| EFXX | W | | | | | D | D | D | D | Output to Custom Microcomputer |
| EFXX | R | | | | | D | D | D | D | Input from Custom Microcomputer |
| Sound Microprocessor Memory Space (IC34) | | | | | | | | | | |
| 0000-0FFF | R | D | D | D | D | D | D | D | D | 4K Program ROM |
| 4000-43FF | R/W | D | D | D | D | D | D | D | D | 1K Working RAM |
| 6000 | R | D | D | D | D | D | D | D | D | Read DATA from Game Microprocessor |
| 7000 | W | D | D | D | D | D | D | D | D | Write to Sound Chip (GI-AY-3-8910) |
| 8000 | R | D | D | D | D | D | D | D | D | Read from Sound Chip |

Address Decoder



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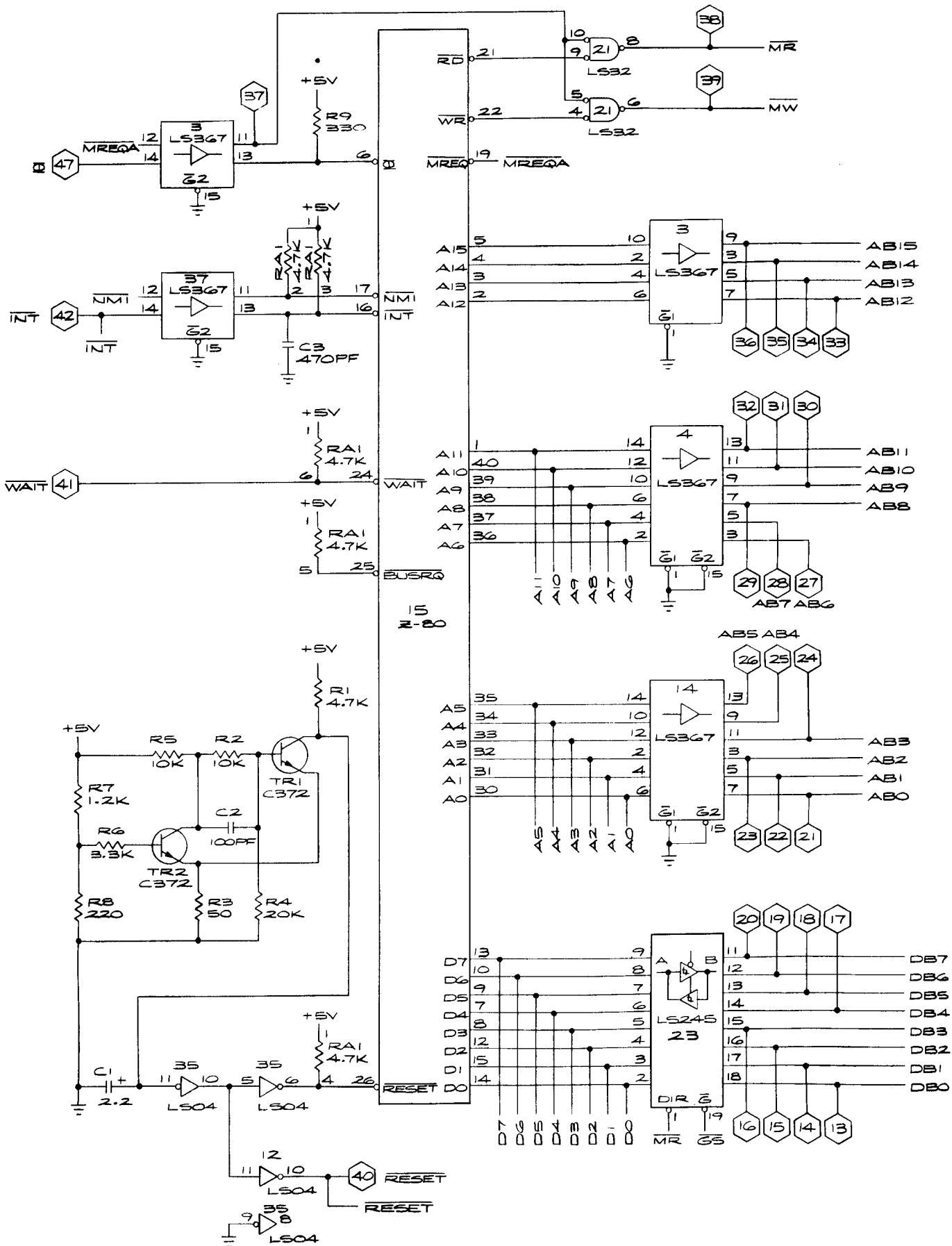
Kangaroo CPU PCB Schematic Diagram

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Game Microprocessor





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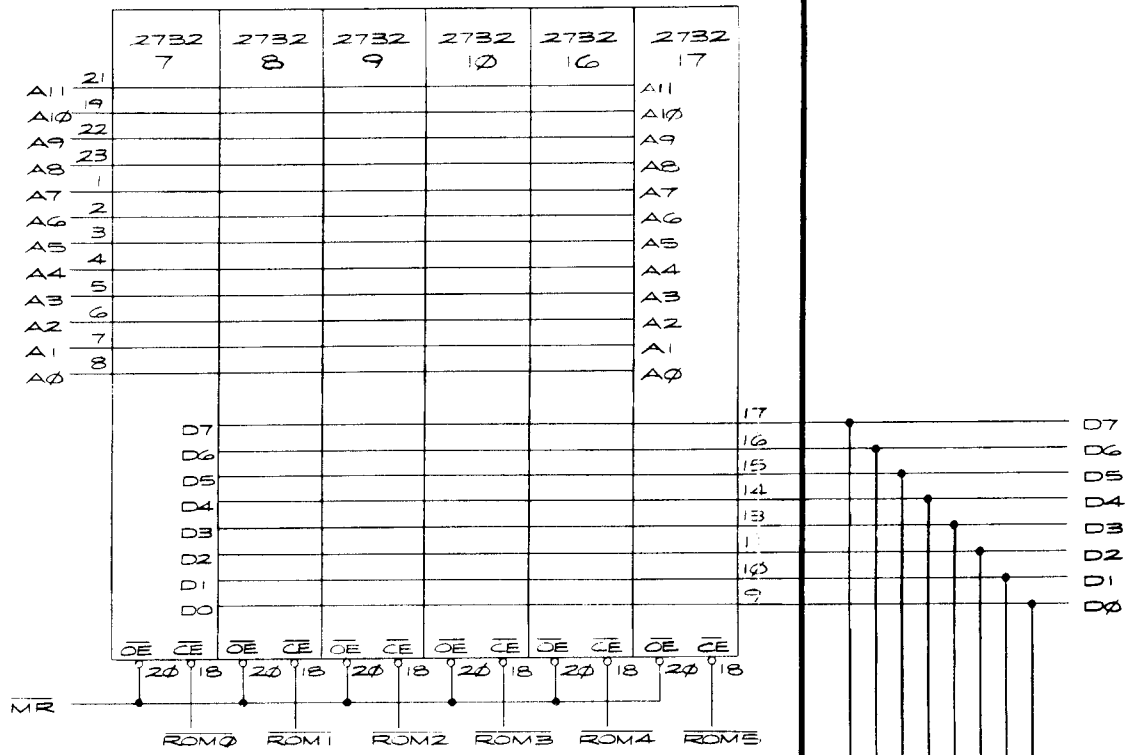
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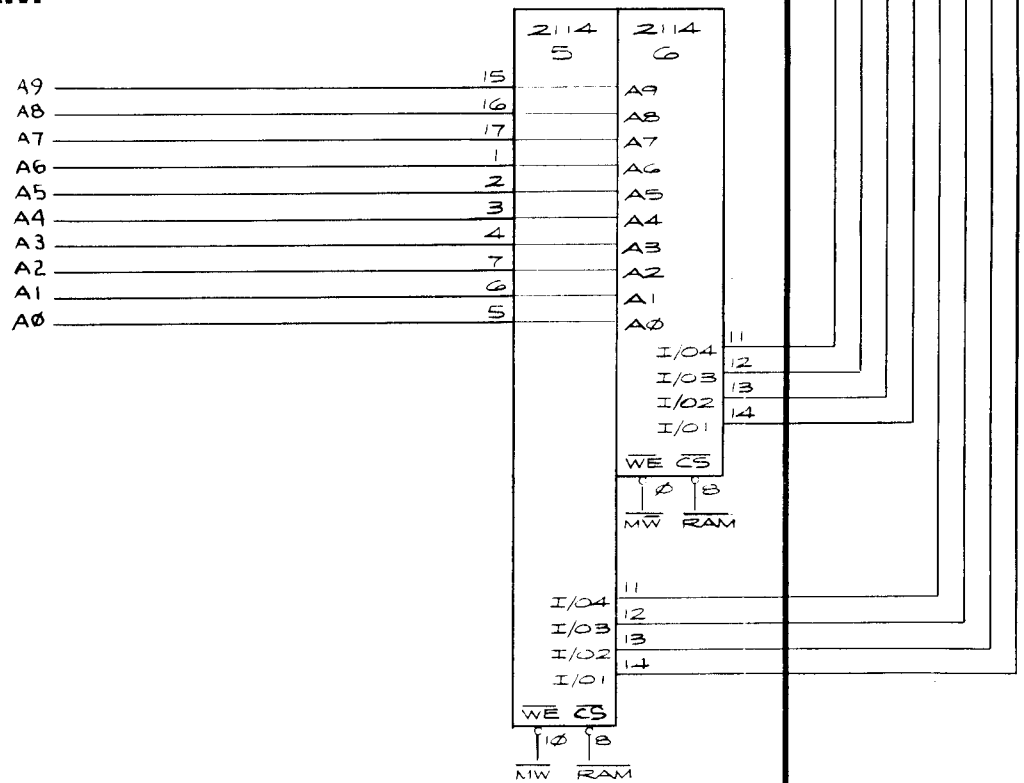
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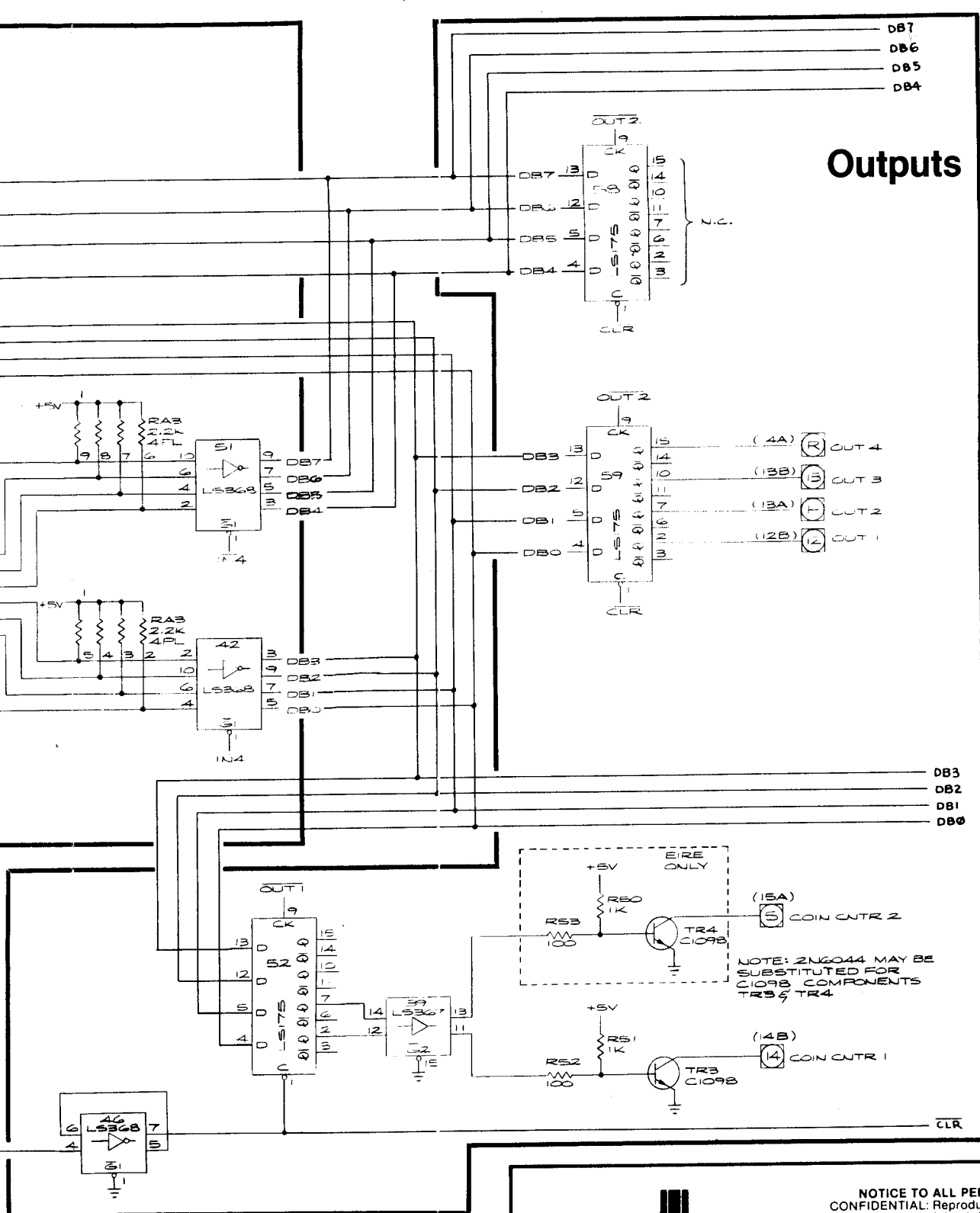
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Program ROM



RAM





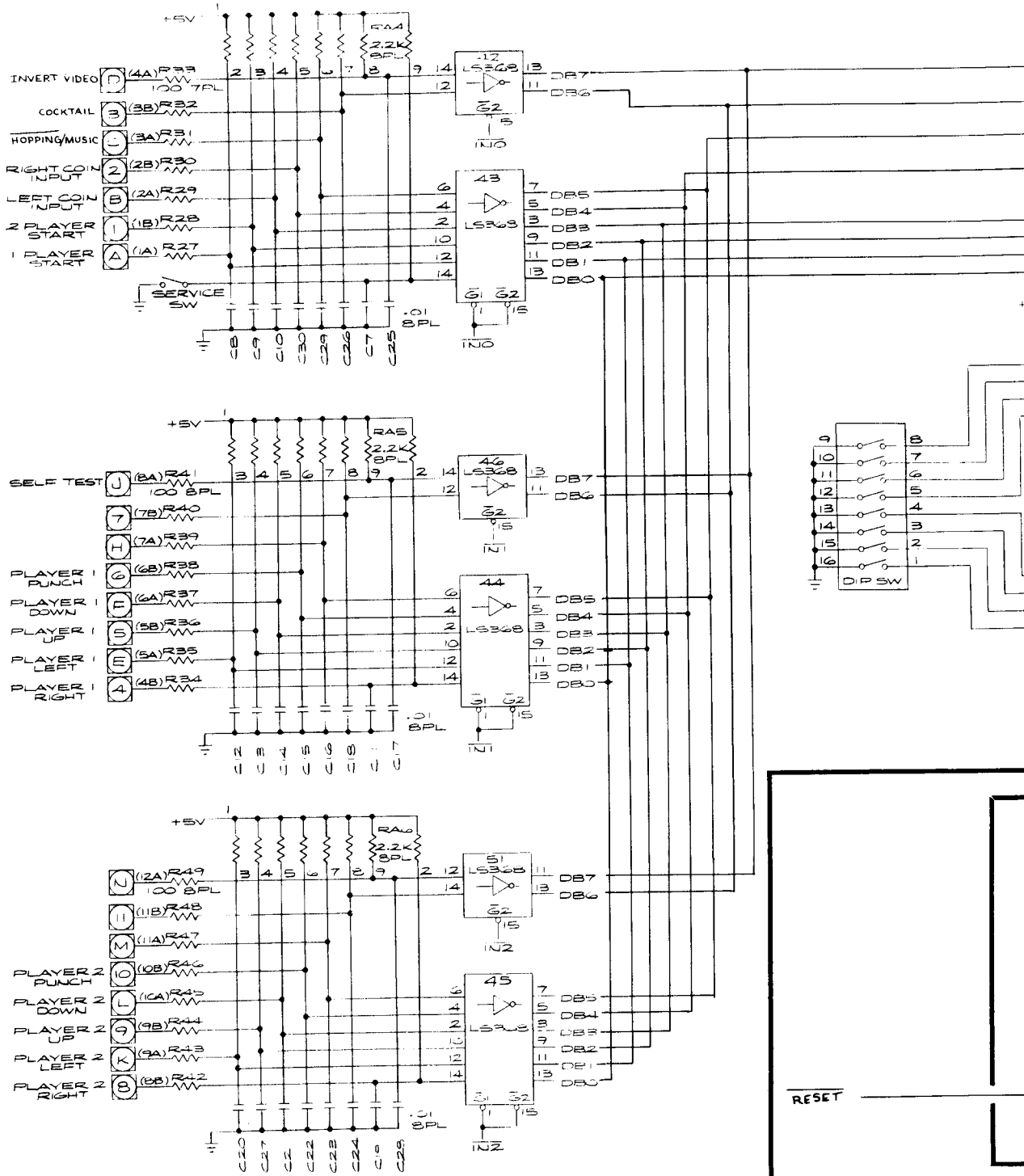
Outputs

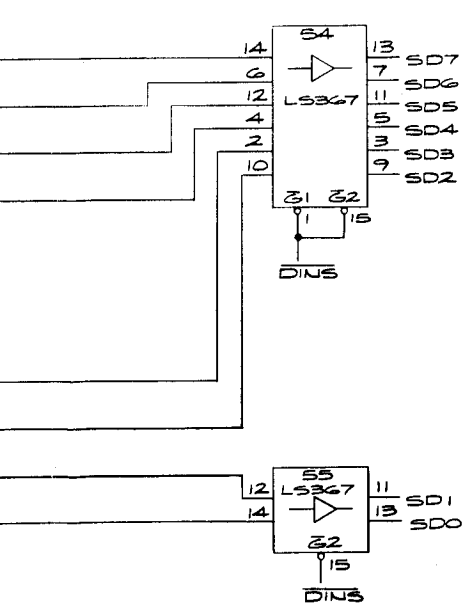
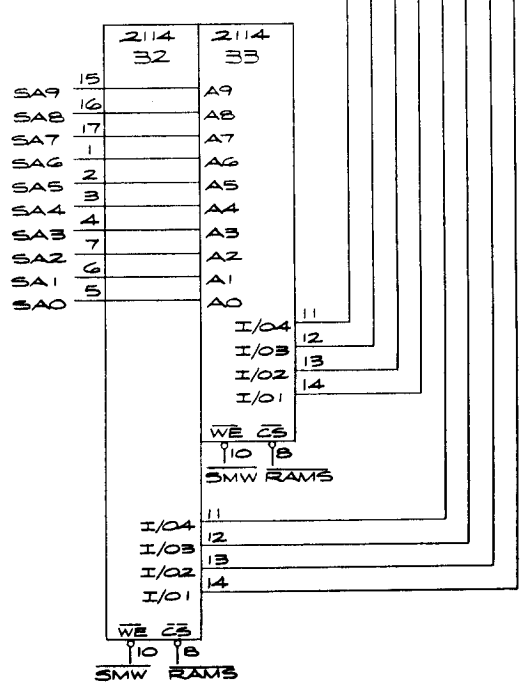
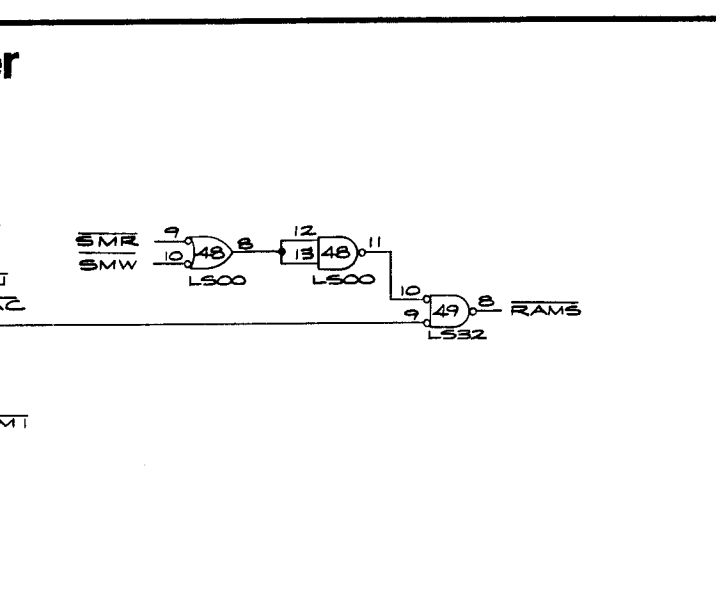
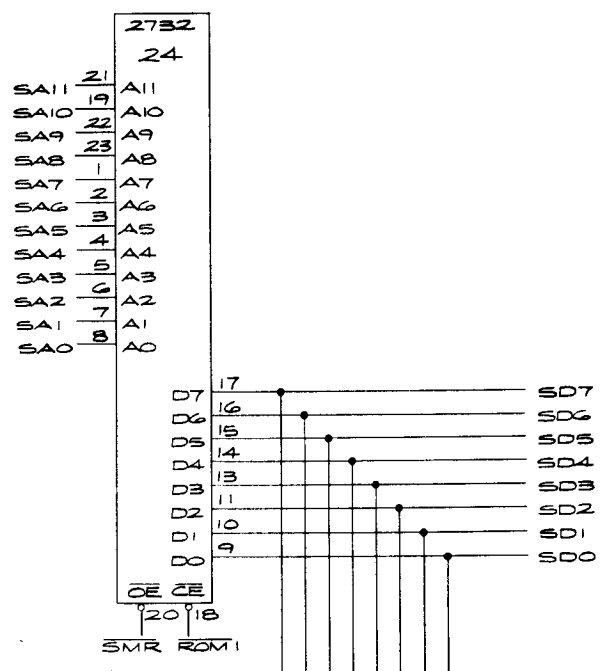
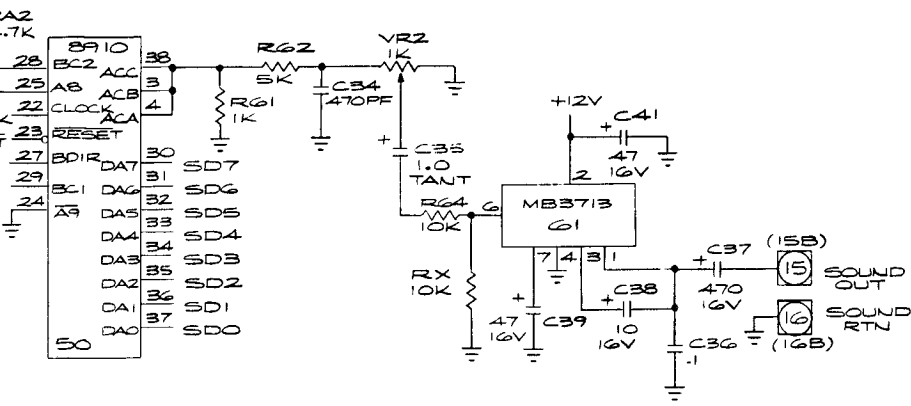
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Kangaroo CPU PCB Schematic Diagram

Inputs







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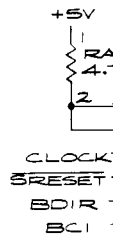
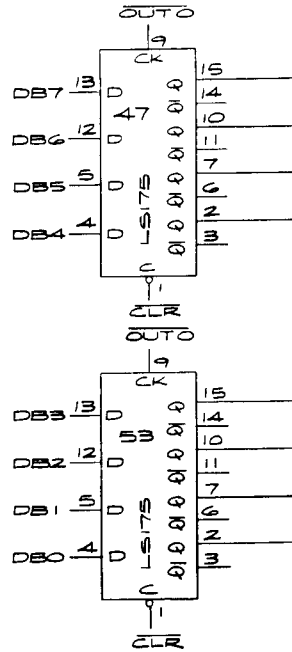
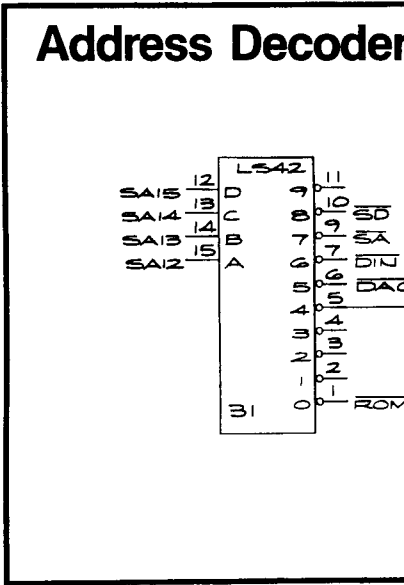
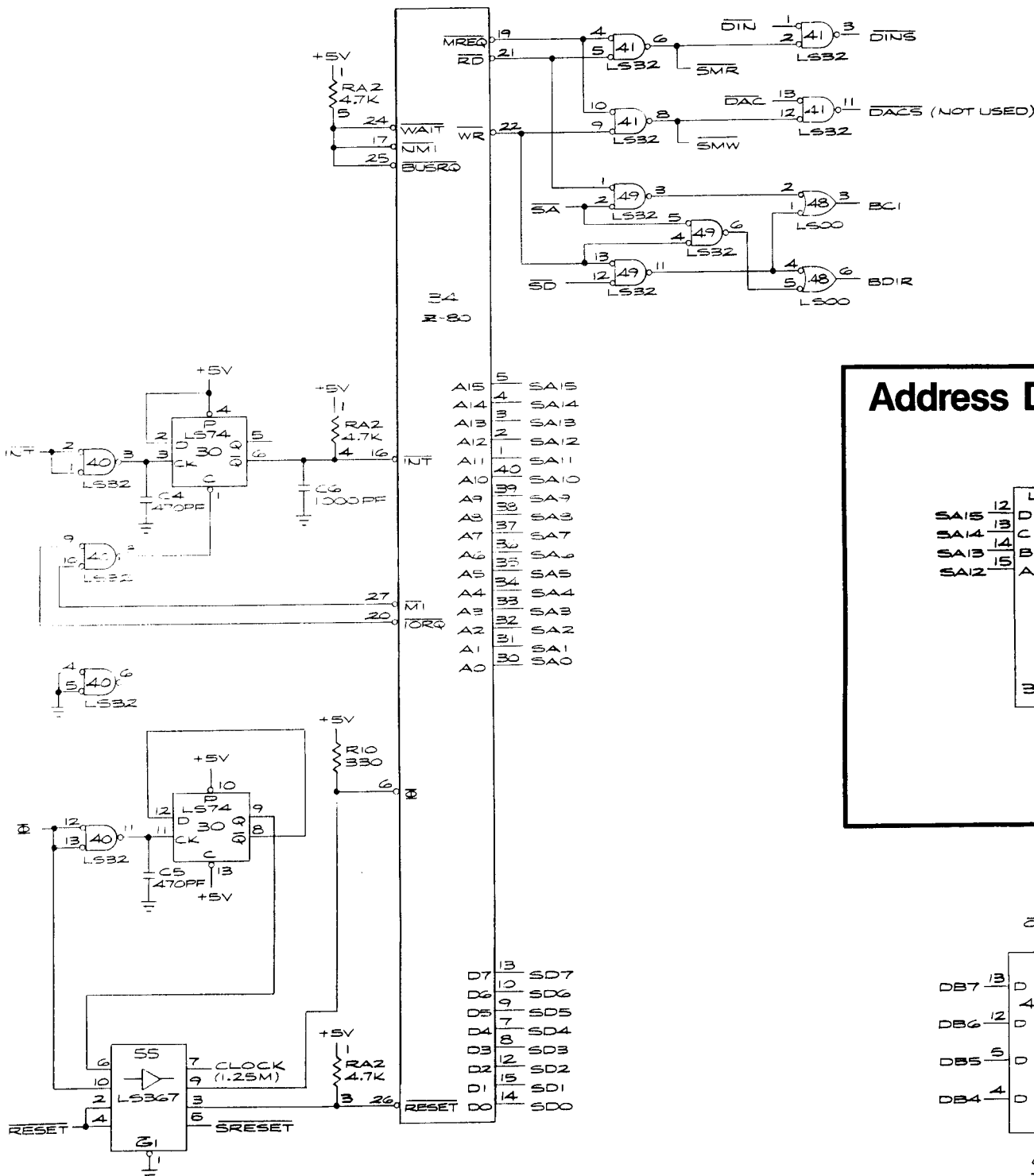
Kangaroo CPU PCB Schematic Diagram

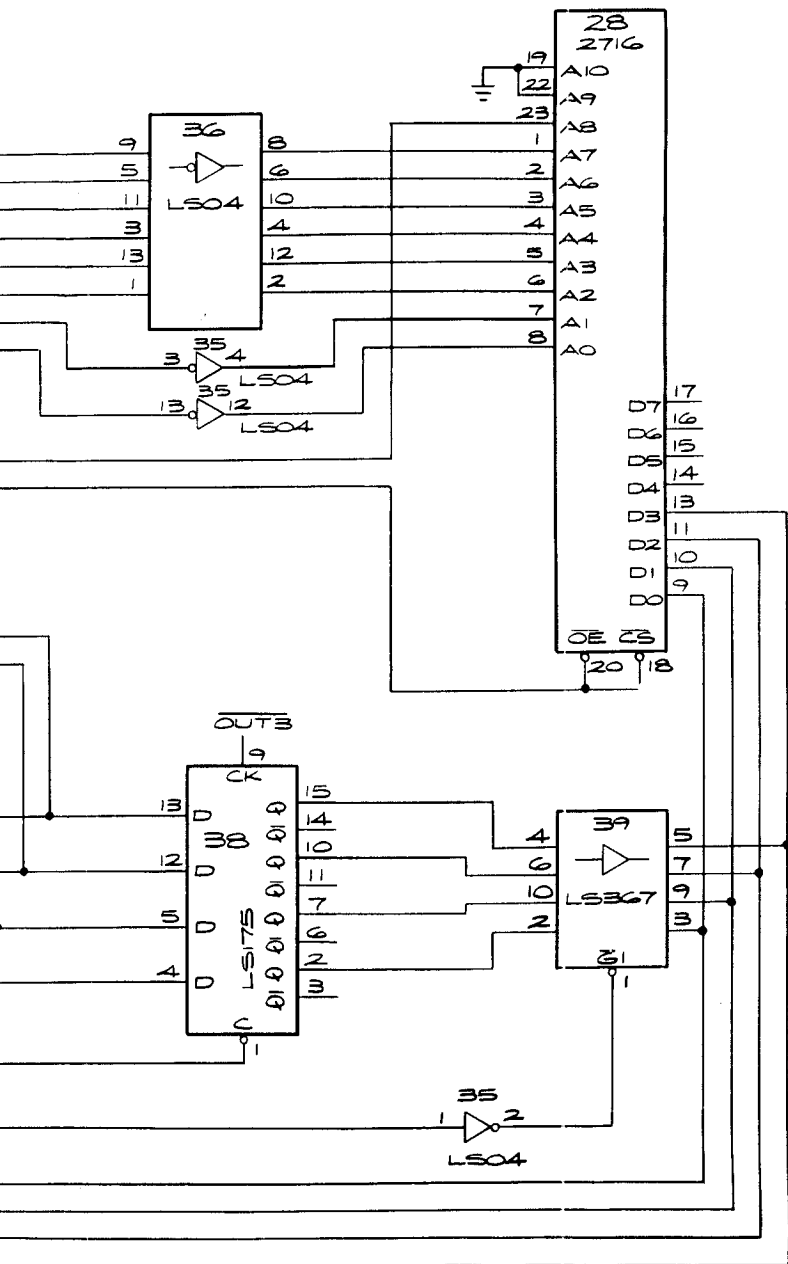
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Sound Microprocessor





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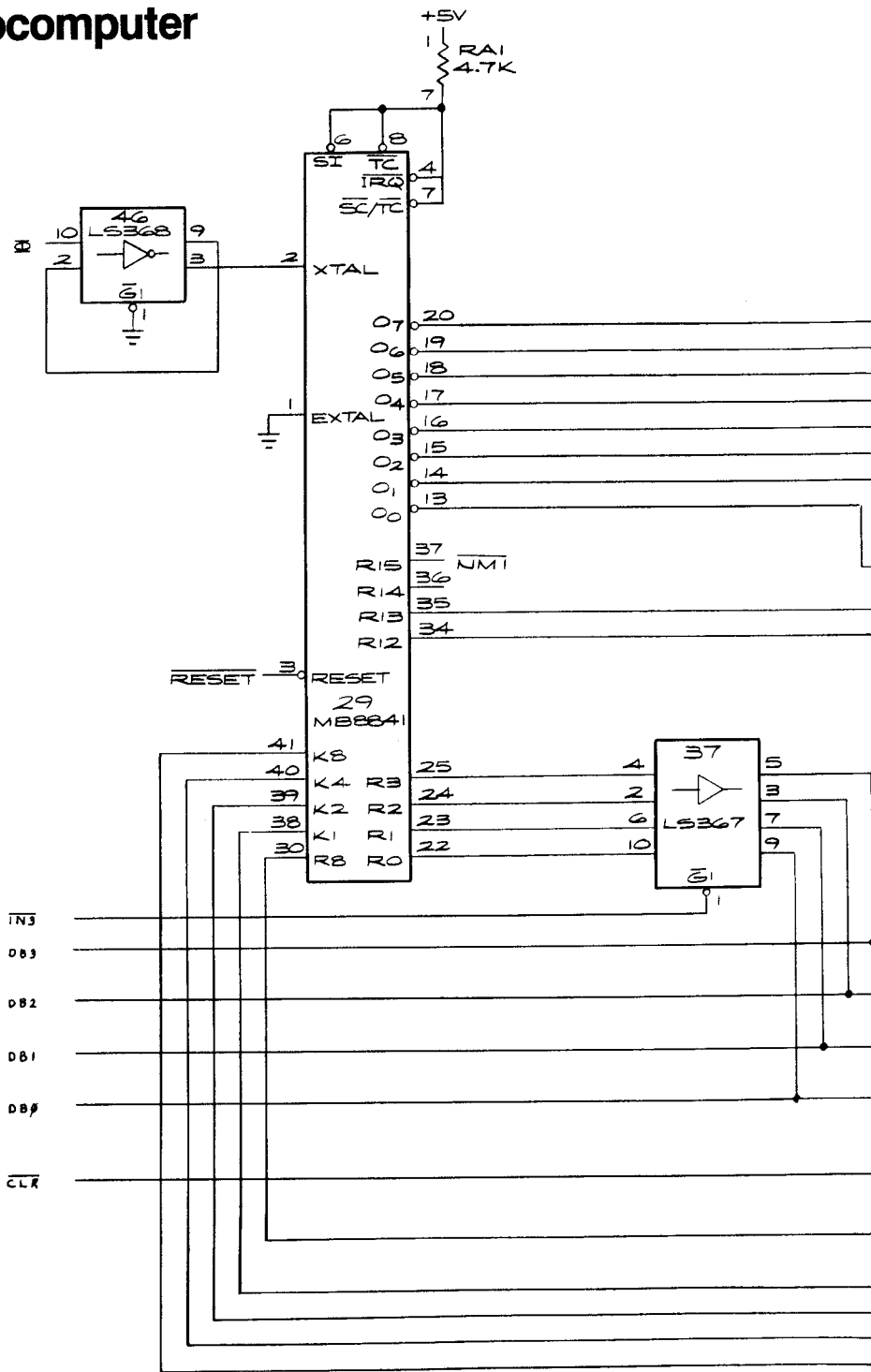
Kangaroo CPU PCB Schematic Diagram

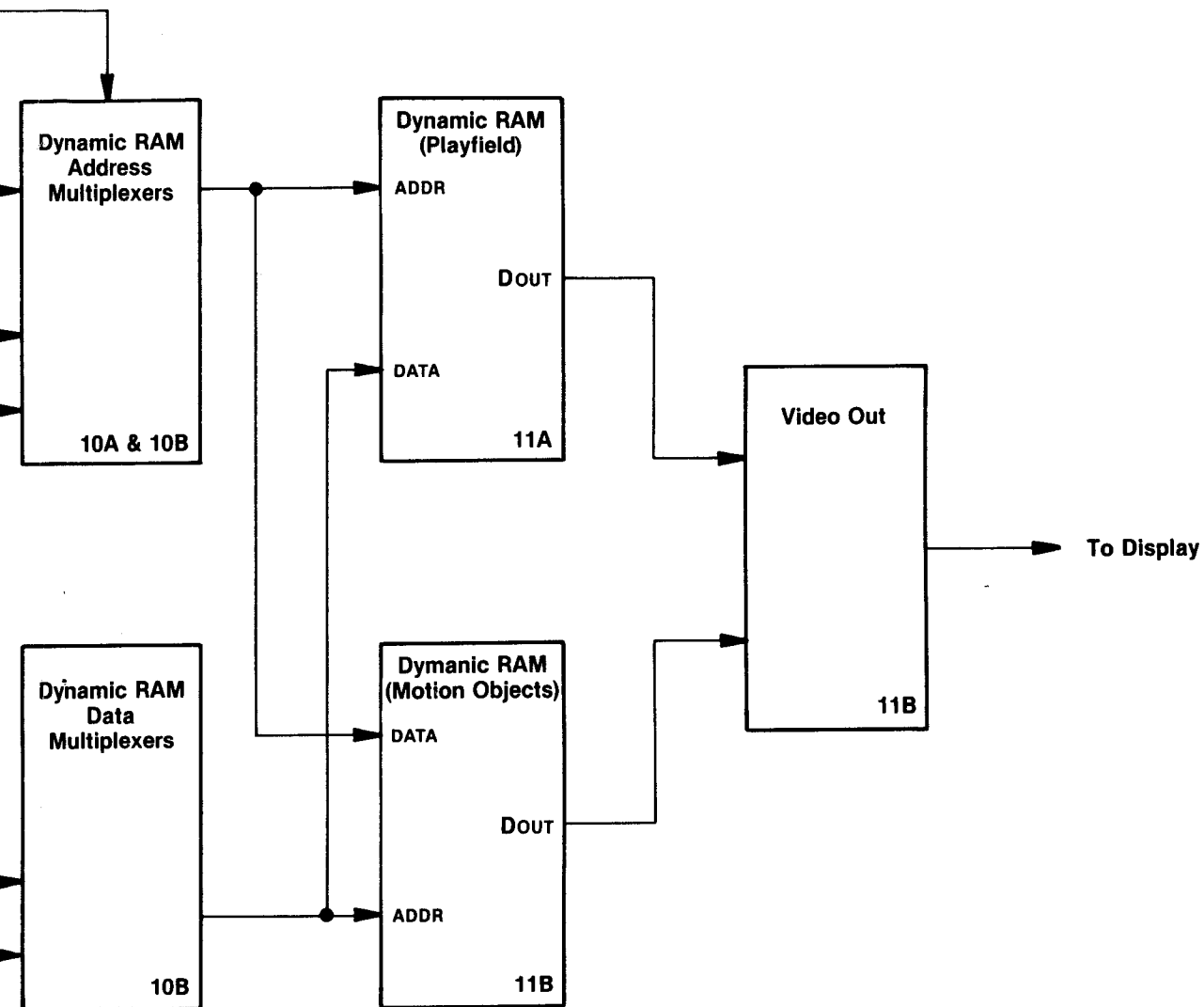
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Custom Microcomputer





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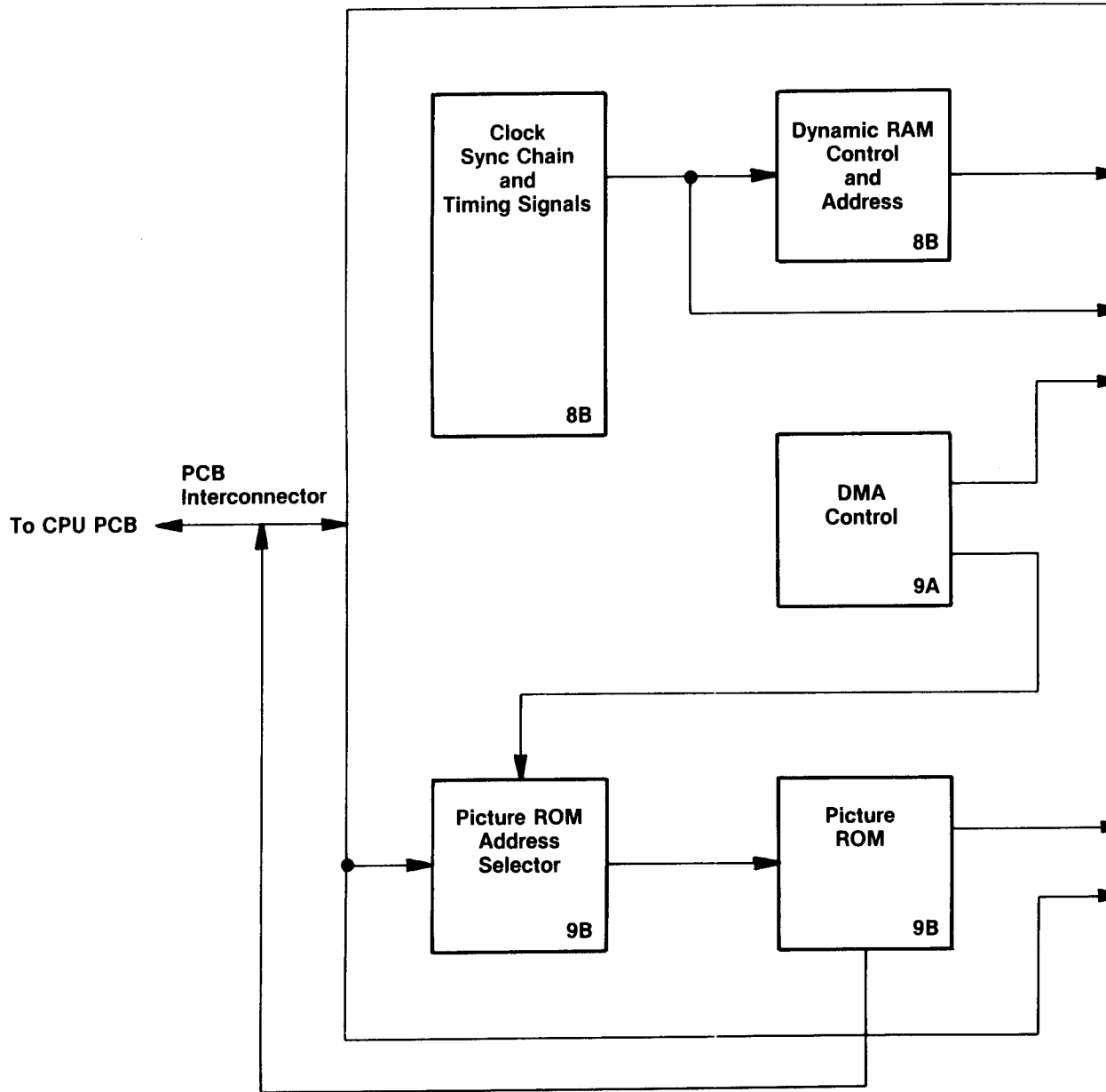
Kangaroo Video PCB Schematic Diagram

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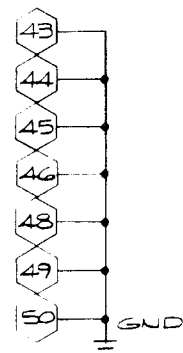
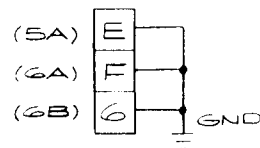
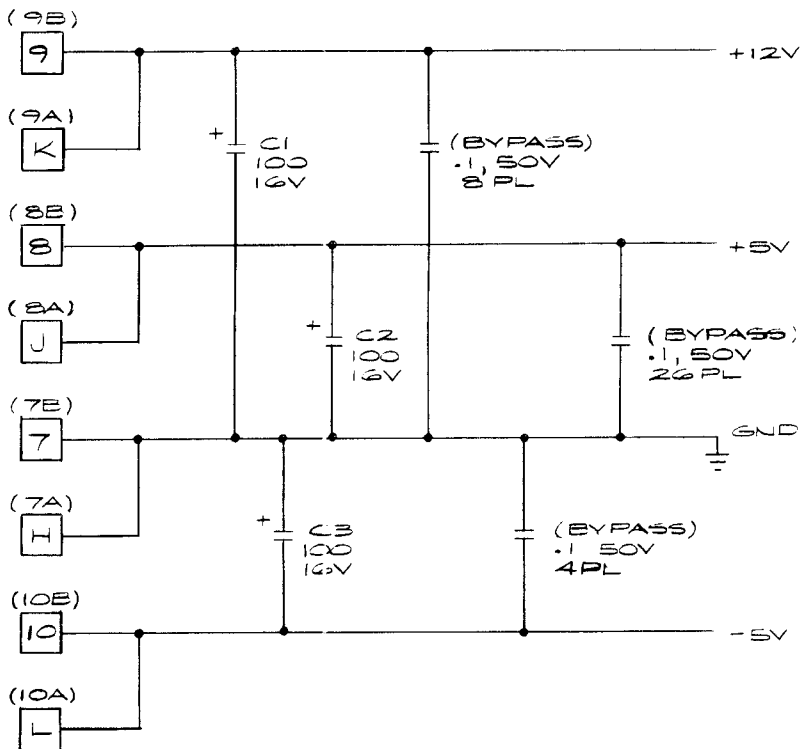
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Block Diagram (Video PCB)



Video Power Input



NOTES:

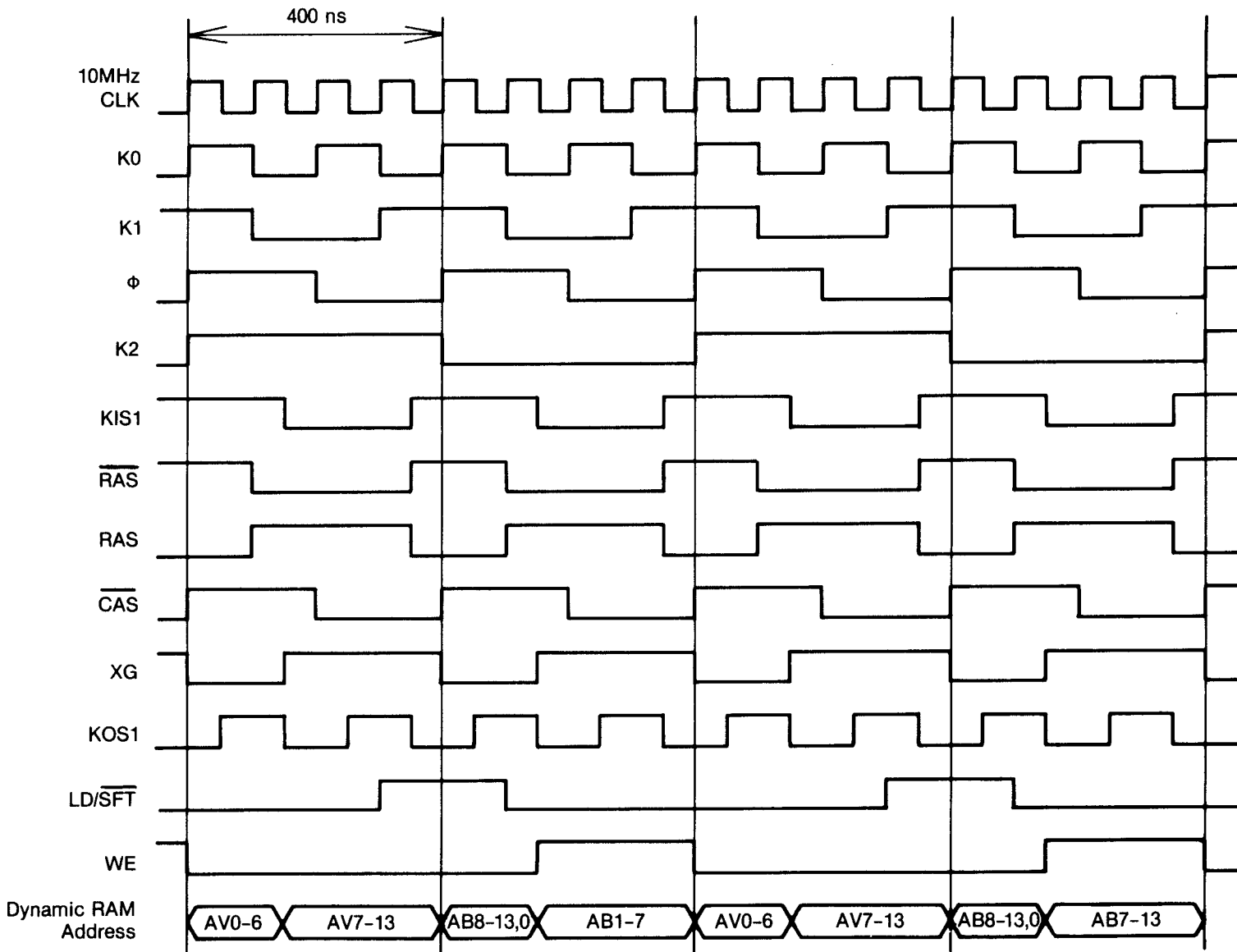
1.  = CONNECTOR CN1
2.  = CONNECTOR CN4



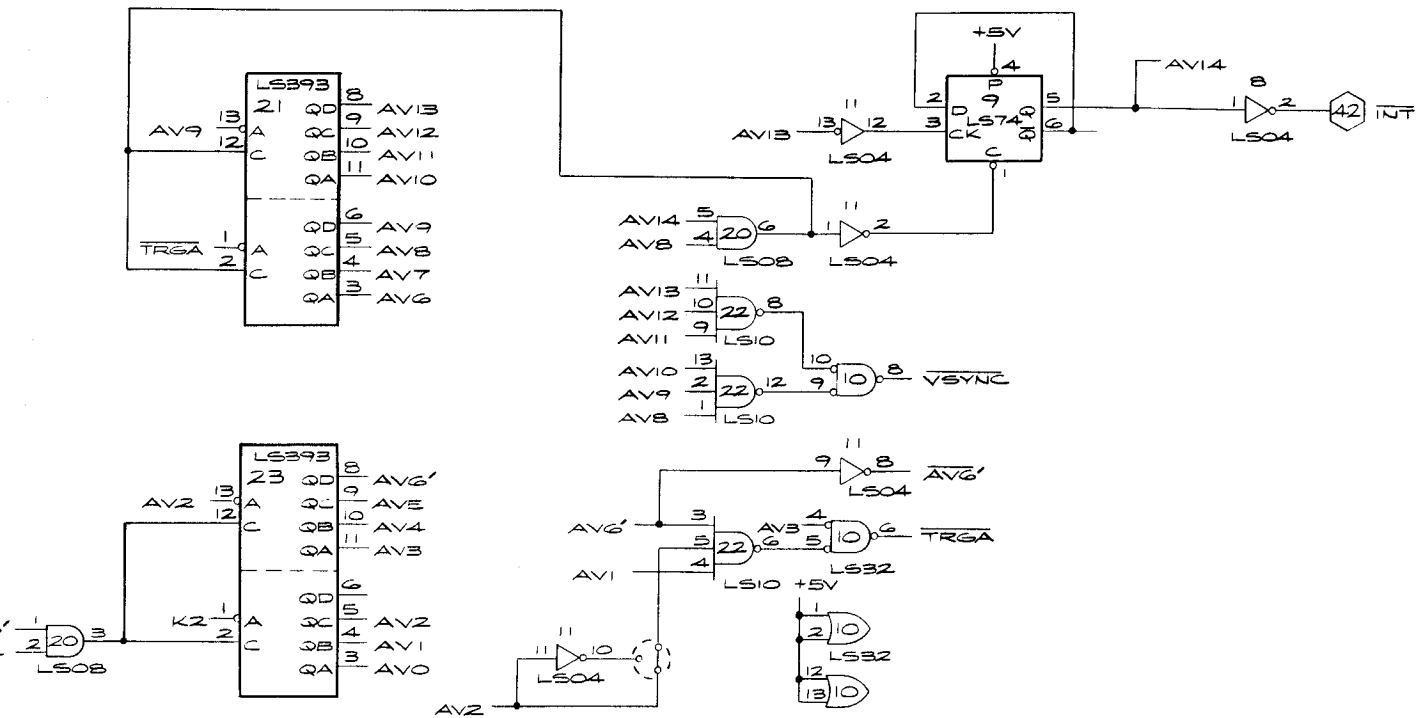
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Kangaroo Video PCB Schematic Diagram

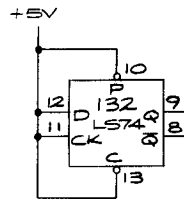
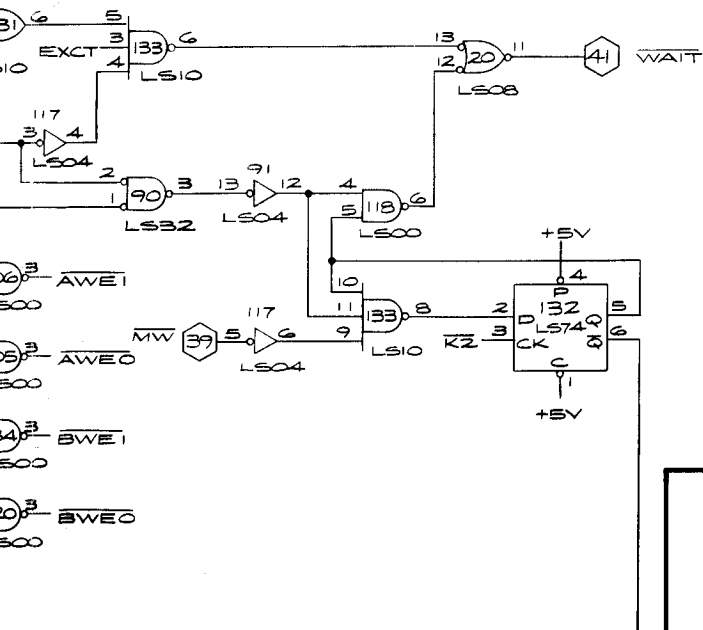
Dynamic RAM Timing Diagram (Video PCB)



Timing Signals



Address Decoding



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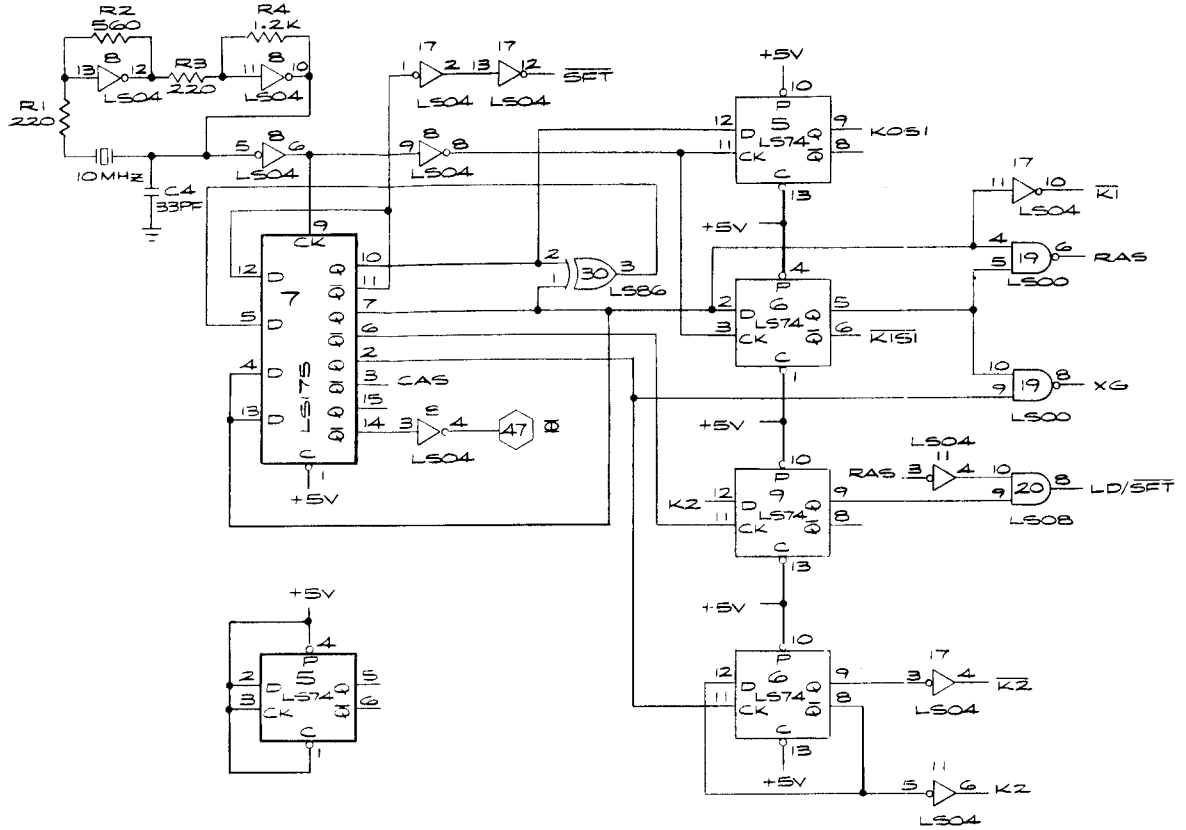
Kangaroo Video PCB Schematic Diagram

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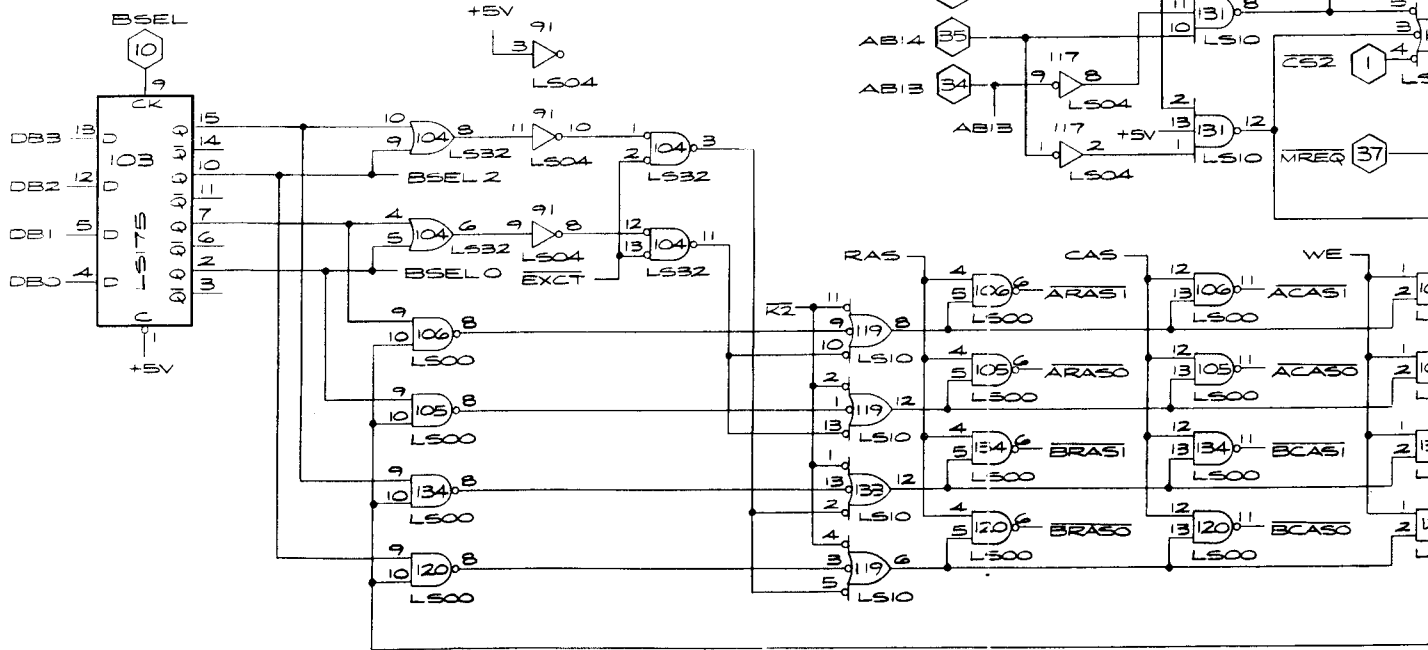
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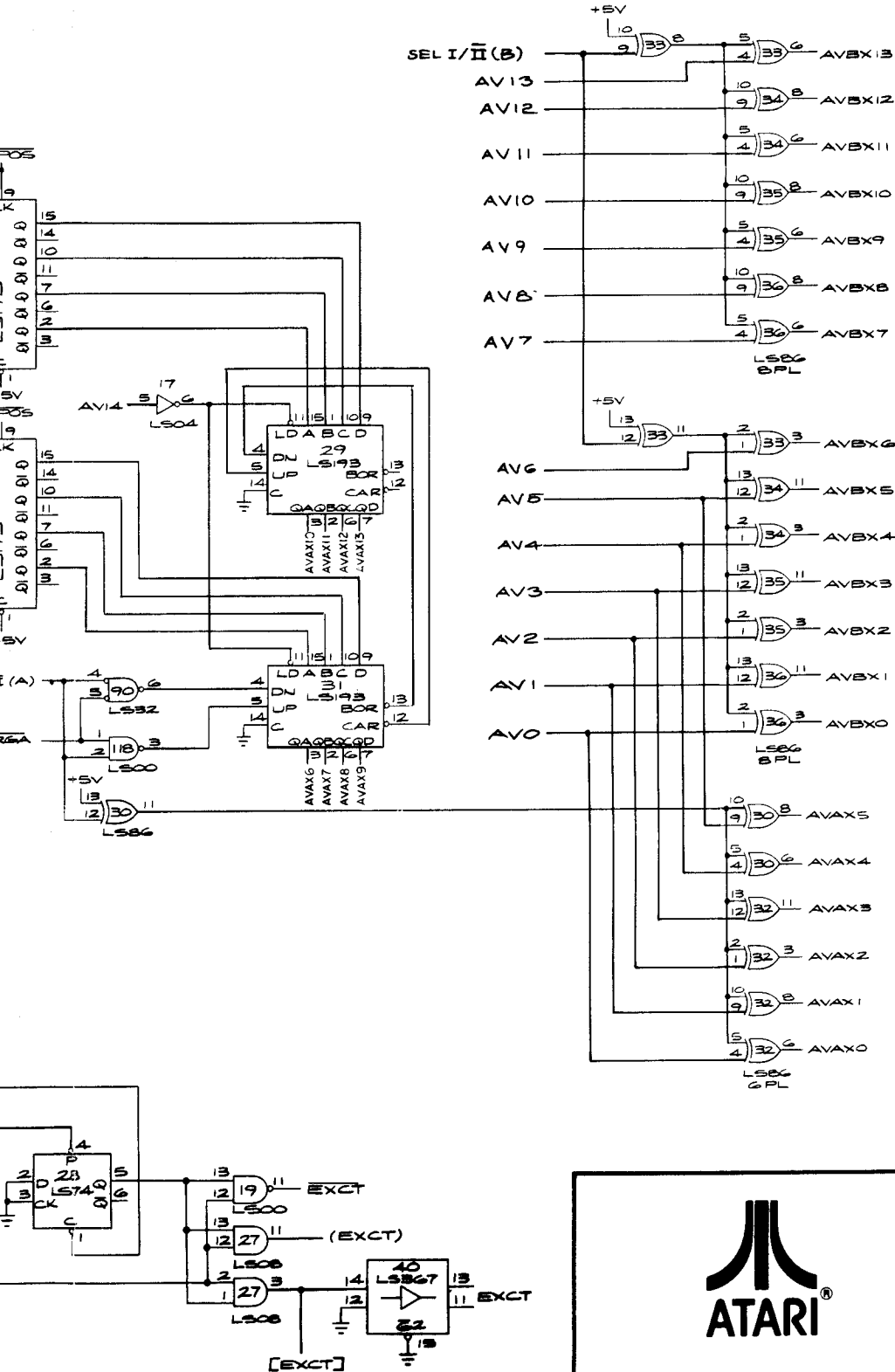
Clock, Sync Chain, a



Dynamic RAM Control



Dynamic RAM Video Address and Flip



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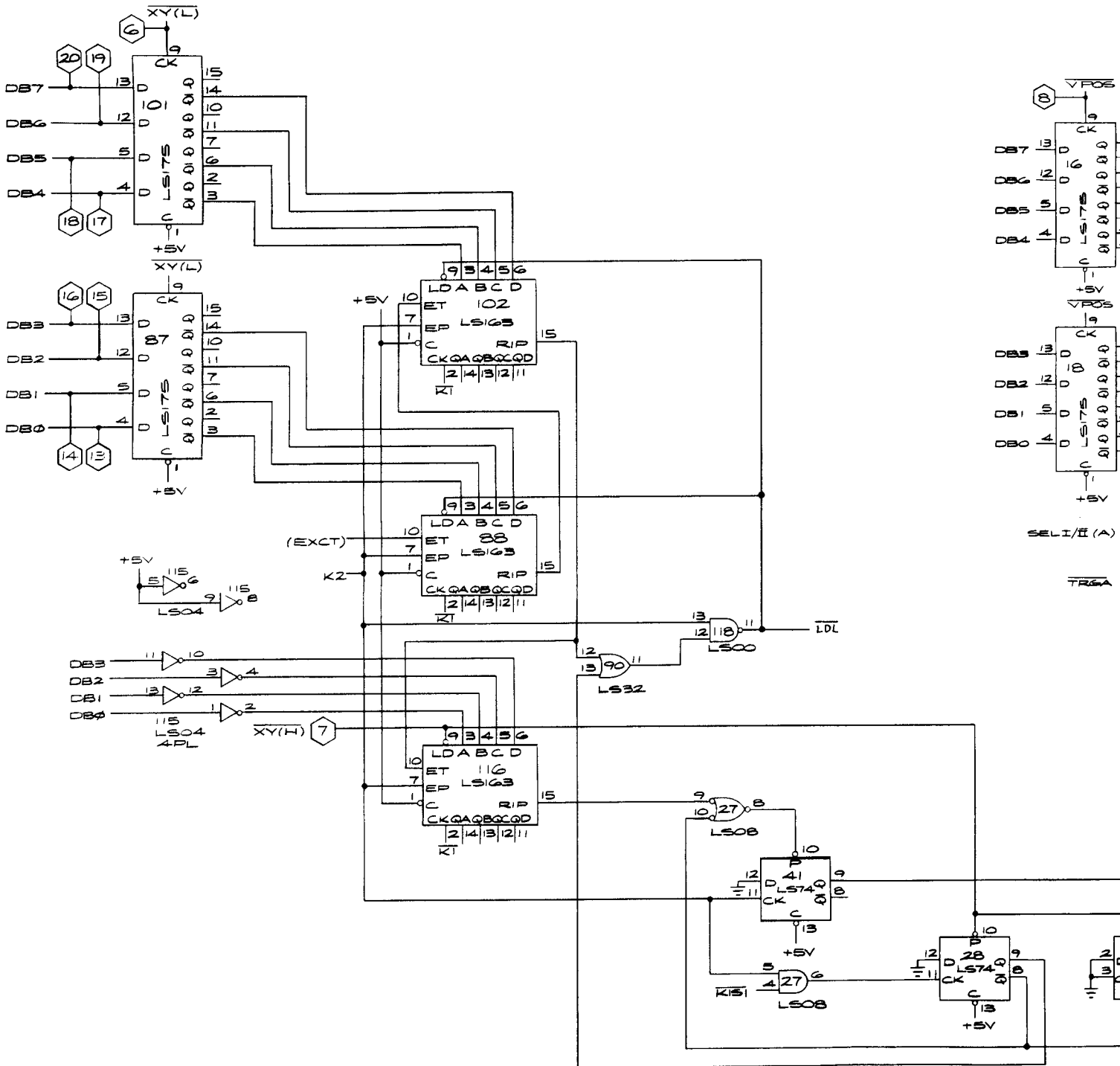
Kangaroo Video PCB Schematic Diagram

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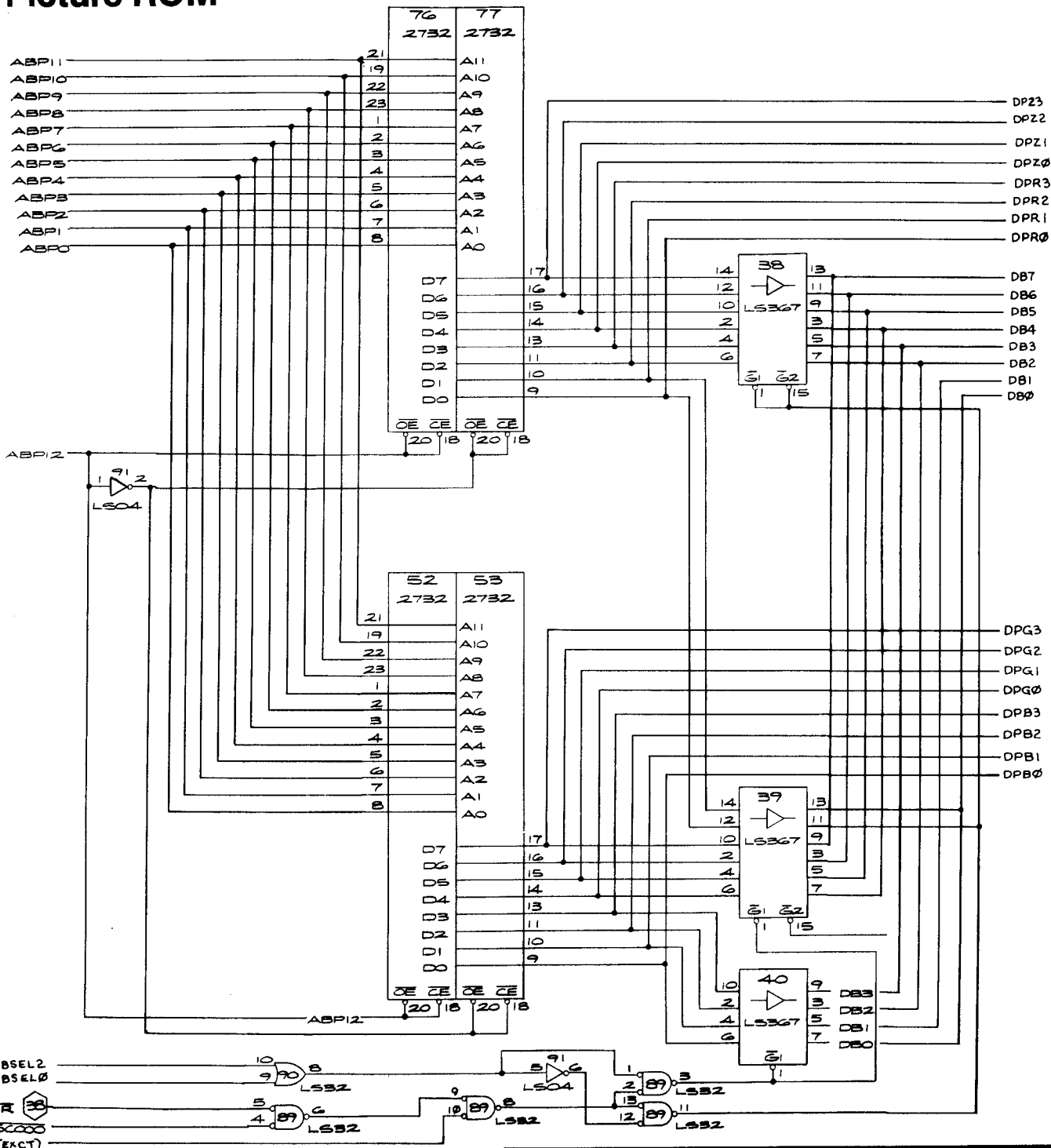
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DMA Control



Picture ROM



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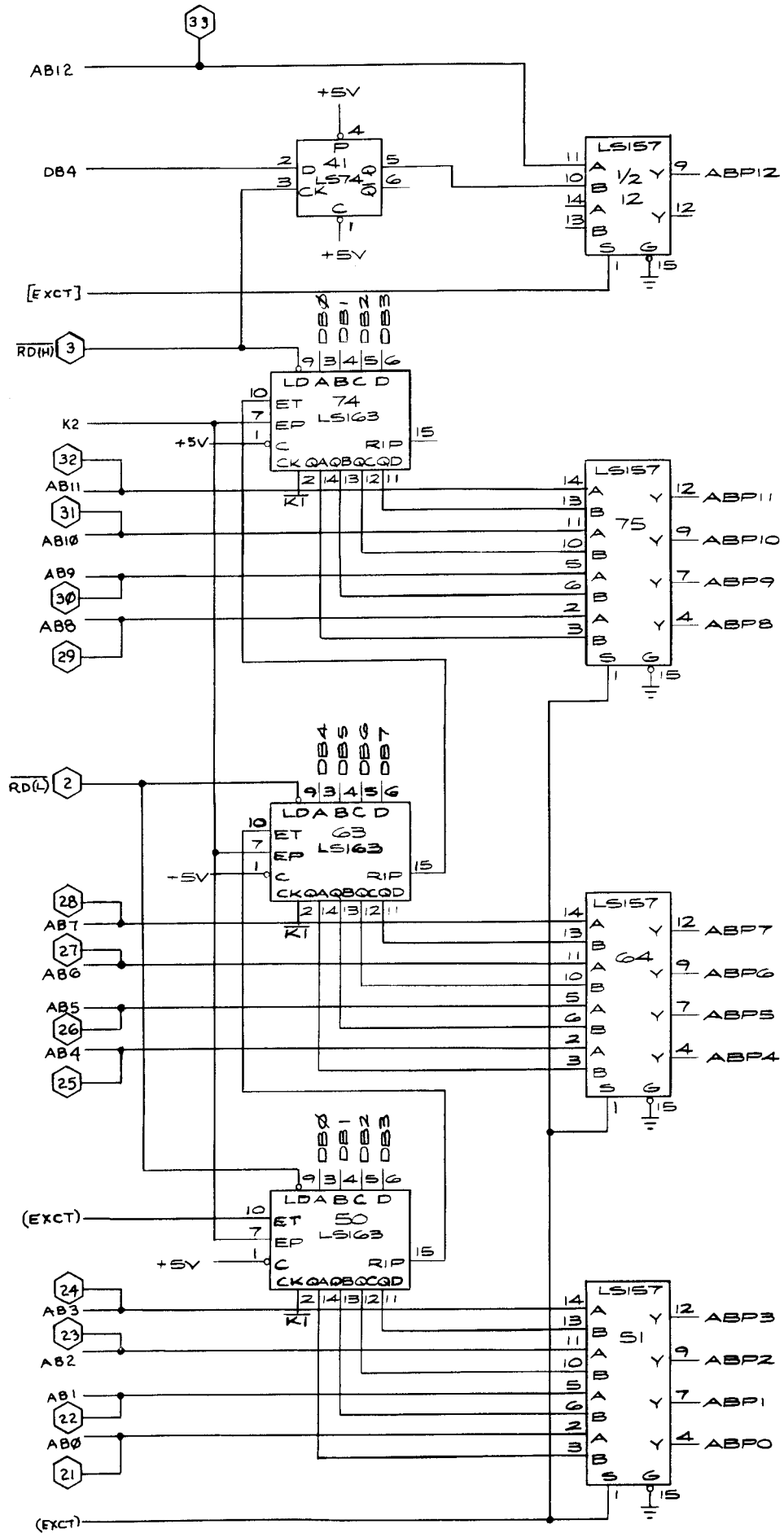
Kangaroo Video PCB Schematic Diagram

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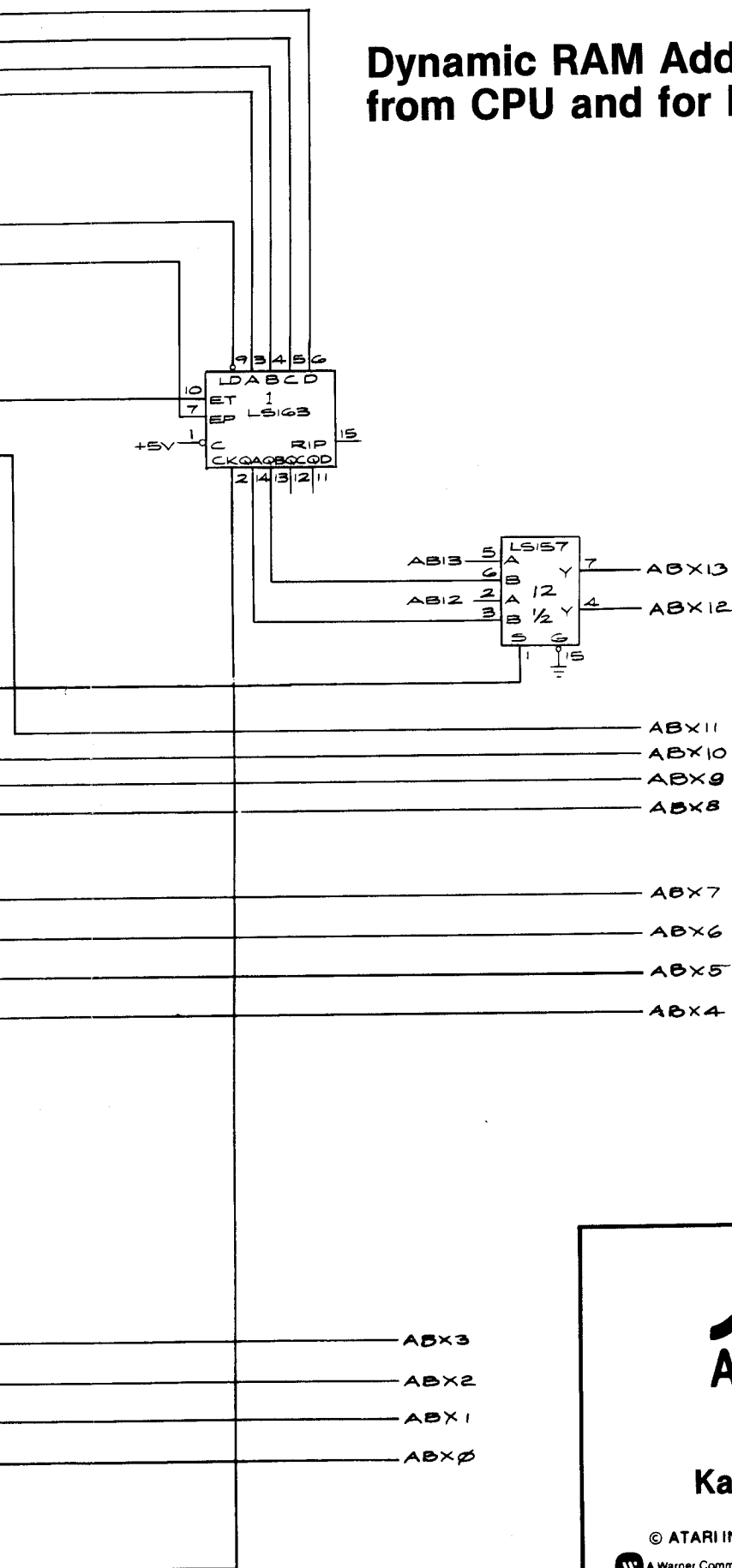
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Picture ROM Address Selector



Dynamic RAM Address from CPU and for DMA



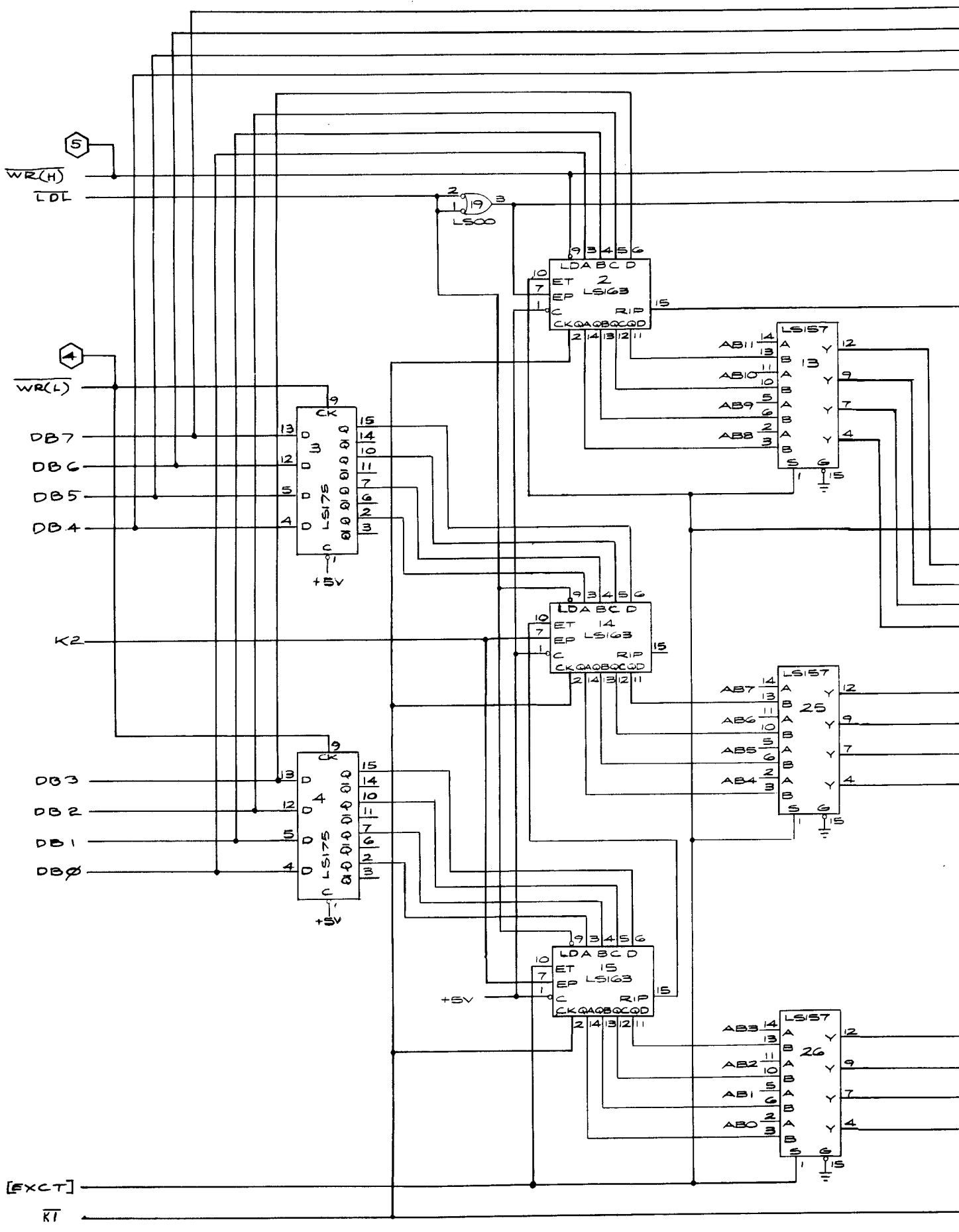
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Kangaroo Video PCB Schematic Diagram

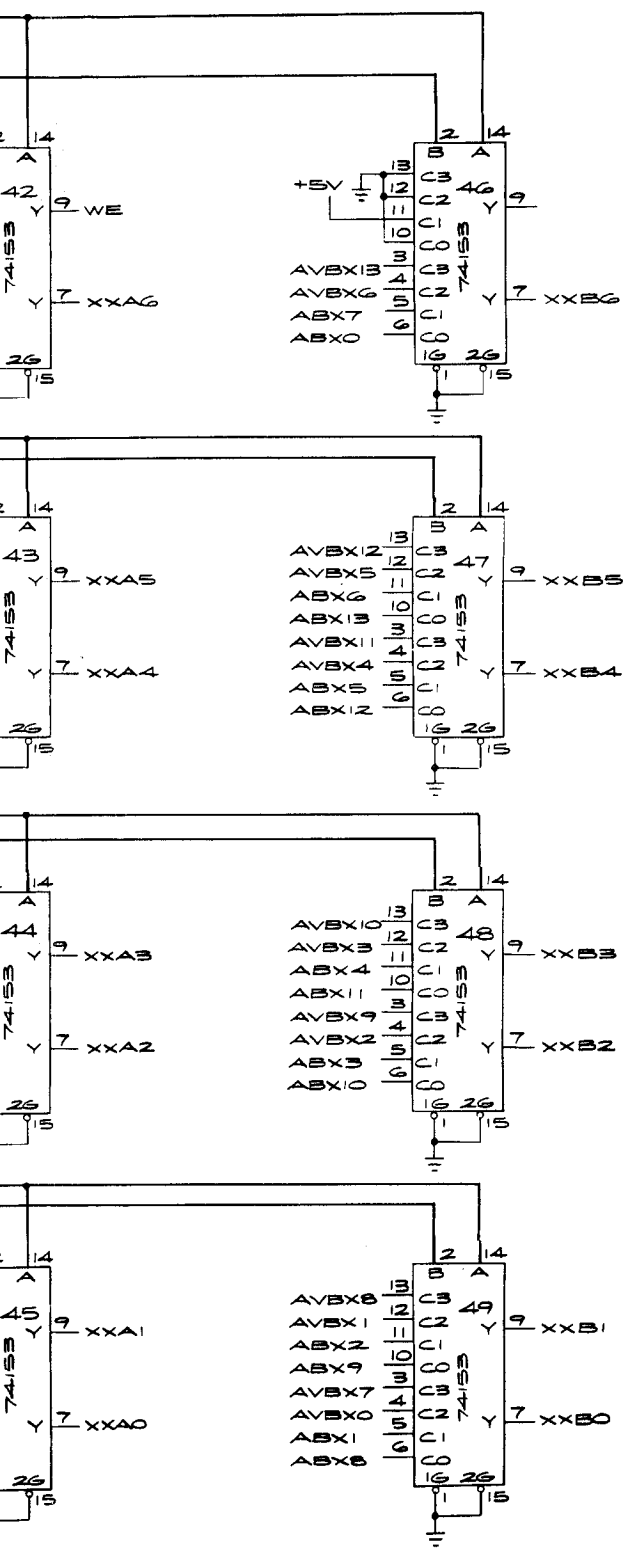
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Address Selector



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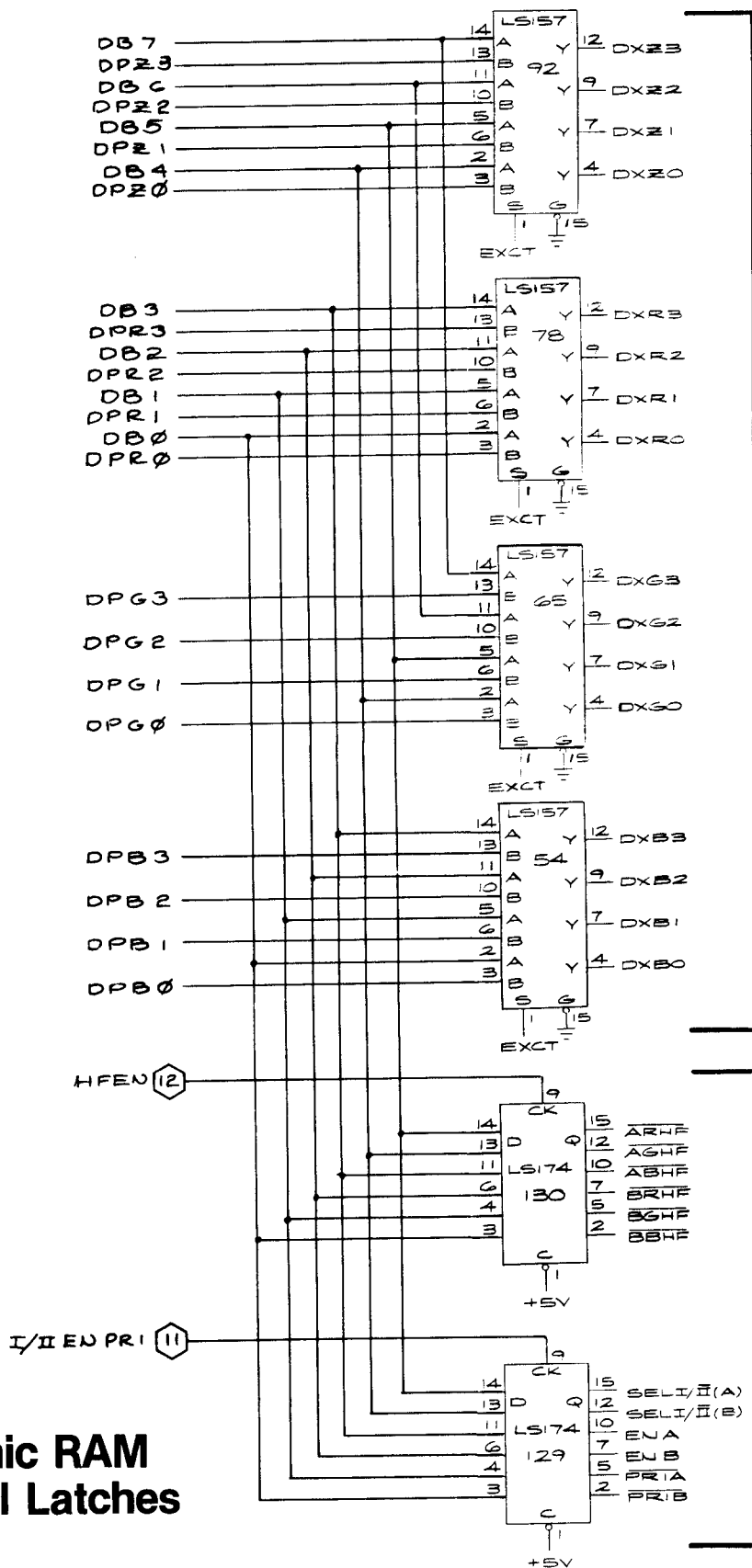
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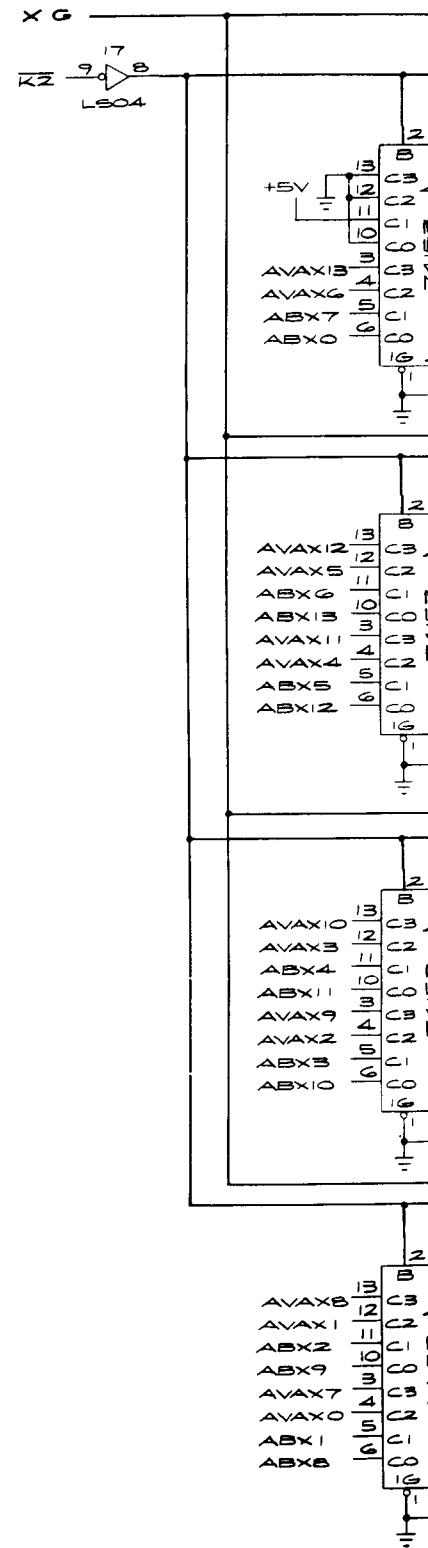
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Dynamic RAM Data Selector

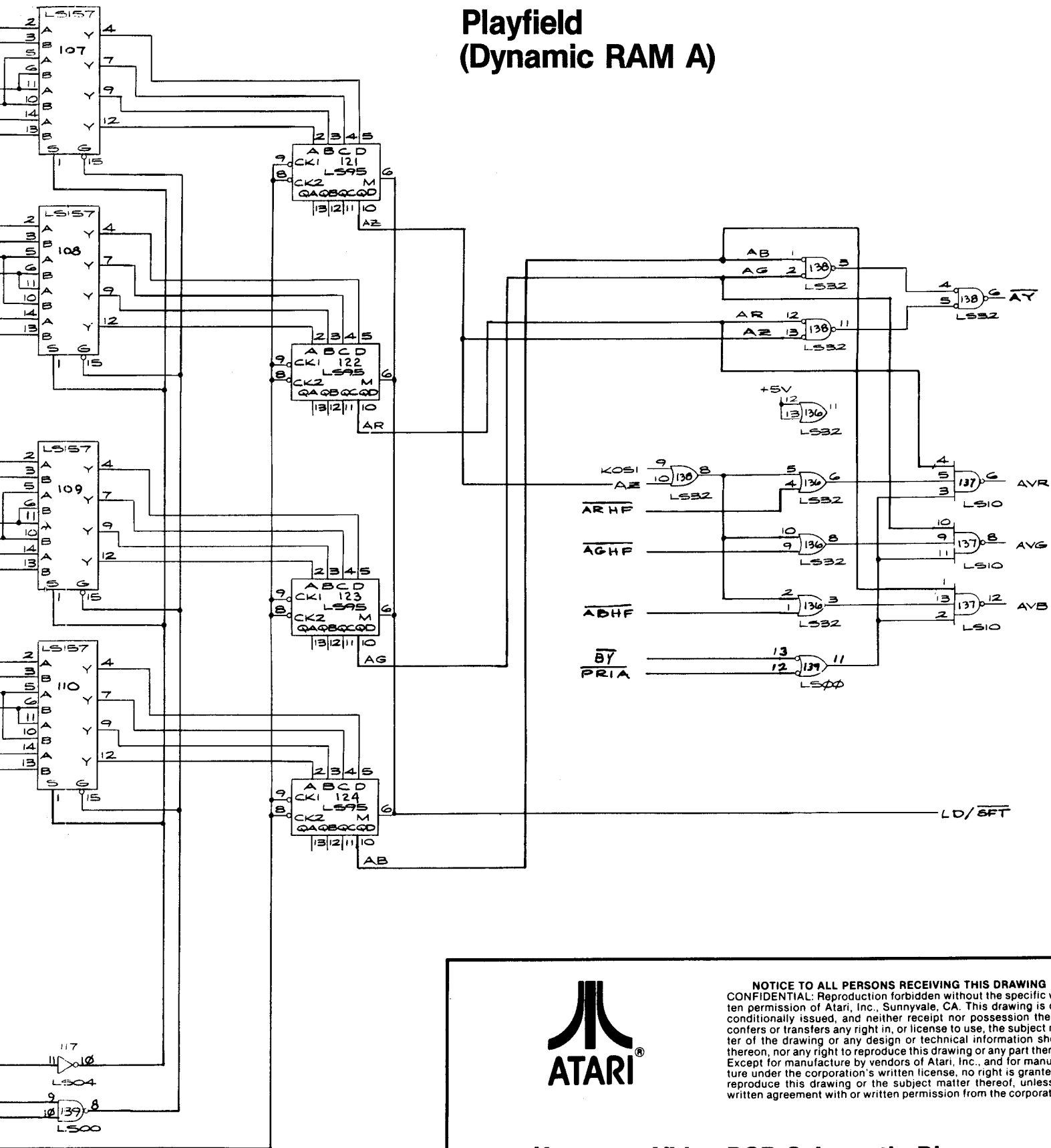
Dynamic RAM



Dynamic RAM Control Latches



Playfield (Dynamic RAM A)



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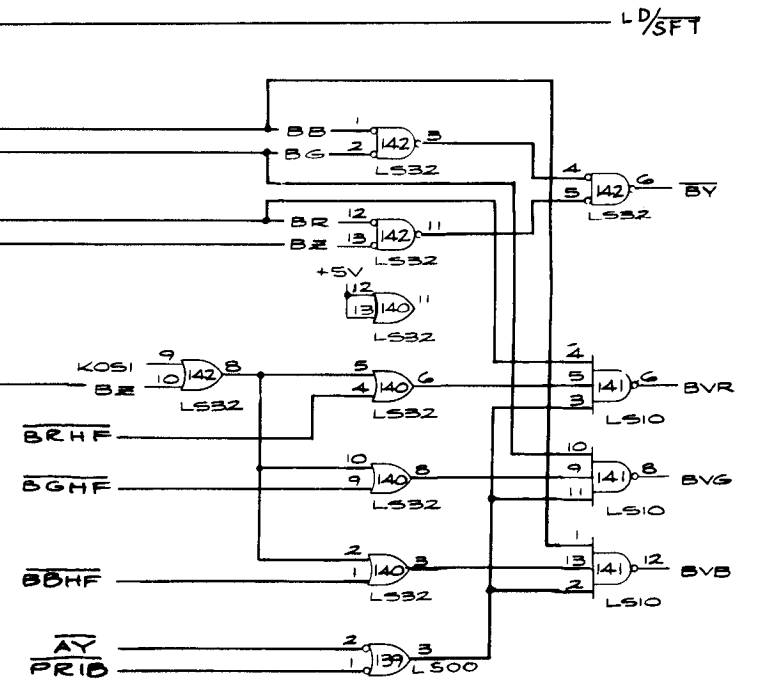
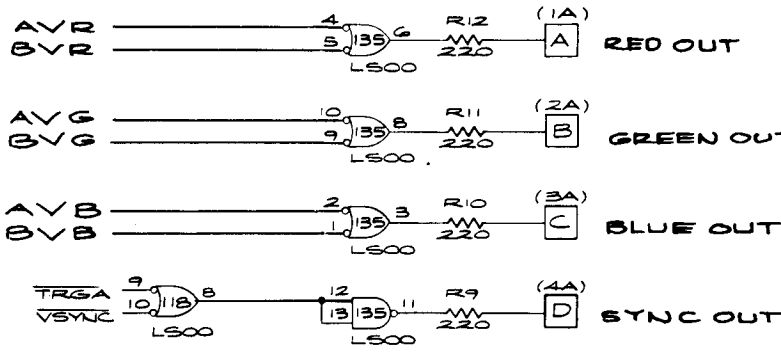
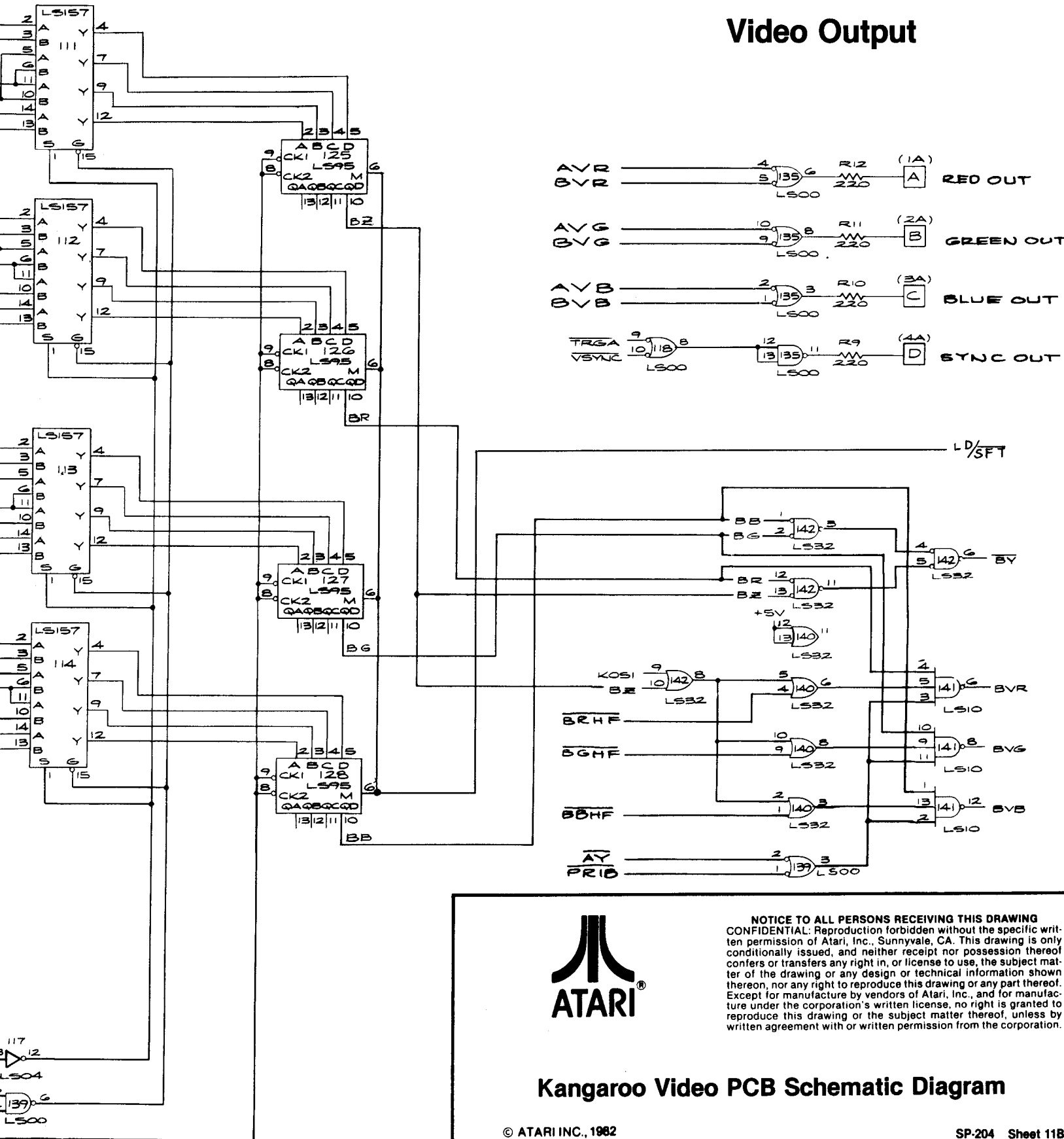
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Video Output



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Kangaroo Video PCB Schematic Diagram

Motion Object (Dynamic RAM B)

