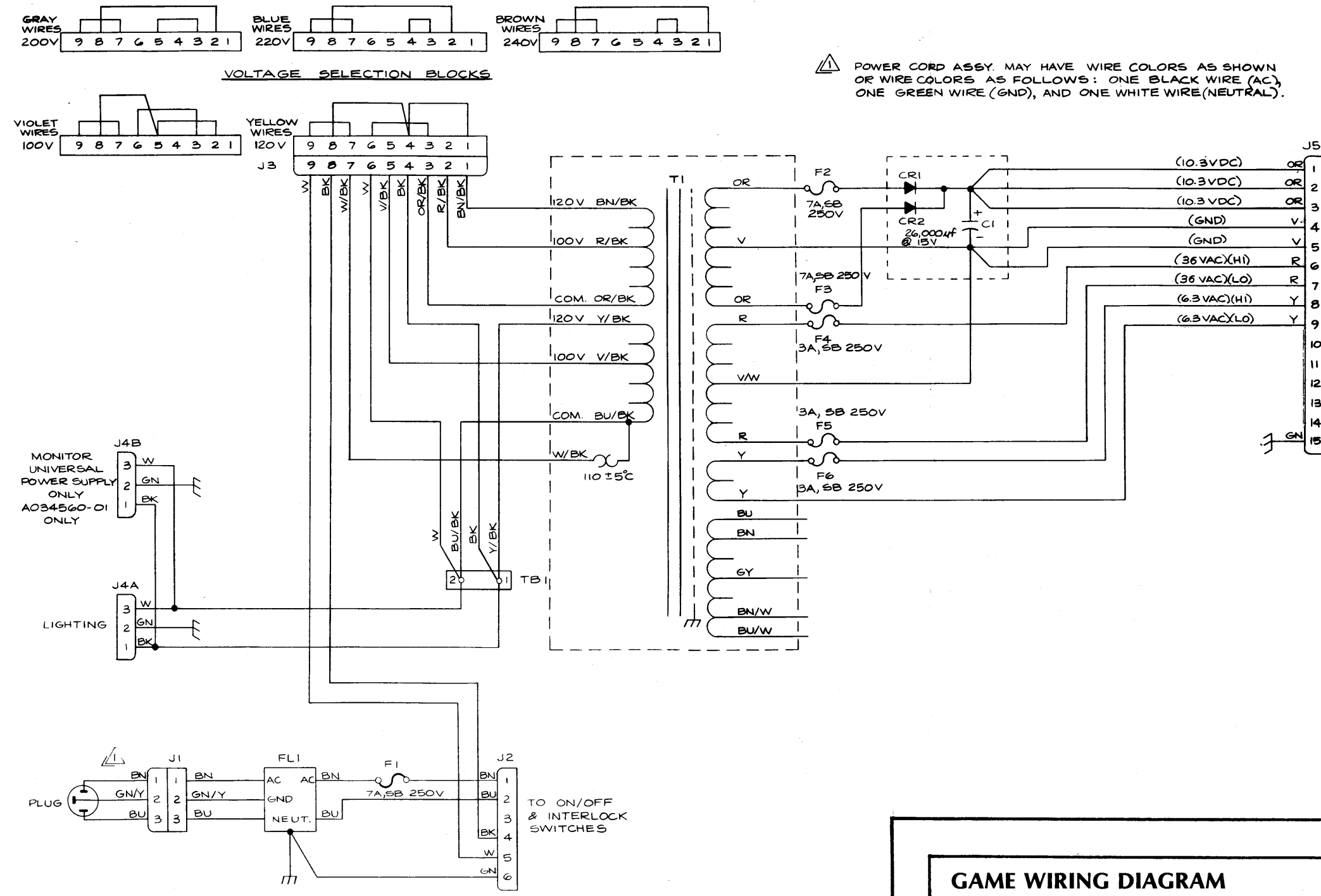


POWER SUPPLY WIRING DIAGRAM (034633-01 A)



REGULATOR/AUDIO PCB SCHEMATIC (034485-01 C)

Regulator/Audio PCB 034485-01 A

The Regulator/Audio PCB has the dual functions of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, current source power transistor Q3 and Q3's bias transistor Q2. The regulator accurately regulates the logic power input to the game PCB by monitoring the voltage through high impedance inputs +SENSE and -SENSE. The inputs are directly from the +5 VDC and ground inputs to the game PCB. Therefore, the regulator regulates the voltage on the game PCB. This eliminates a reduced voltage due to IR buildup on the wire harness between the regulator and the game PCB. Variable resistor R8 is adjusted for the +5 VDC on the game PCB. Once adjusted, the voltage at the input of the game PCB will remain constant at this voltage.

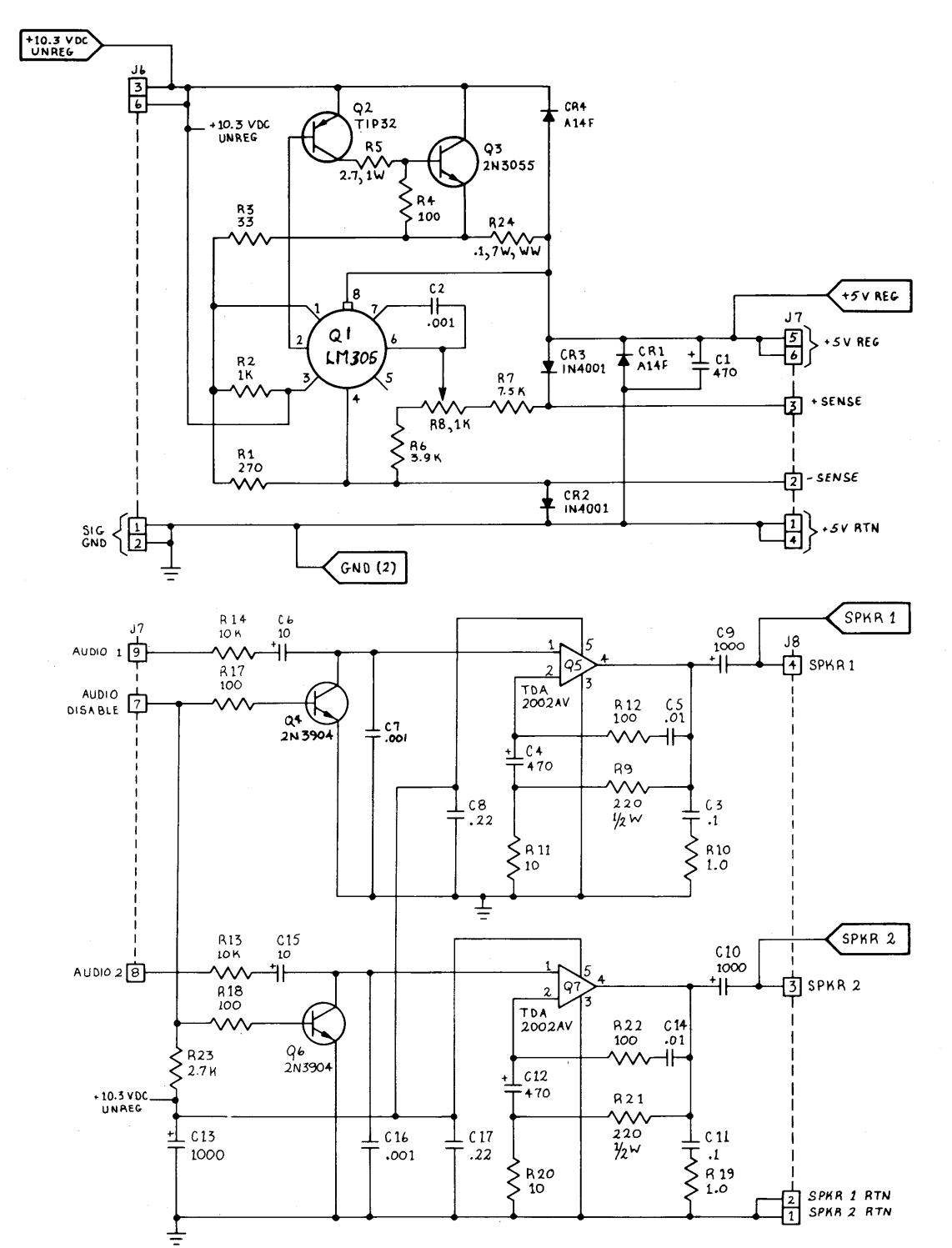
Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test points of the game PCB.
2. Adjust variable resistor R8 on the Regulator/Audio PCB for +5 VDC reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND on the Regulator/Audio PCB. Voltage reading shall not be greater than +5.5 VDC. If greater, try cleaning edge connectors on both the game PCB and the Regulator/Audio PCB.
4. If cleaning PCB edge connectors doesn't decrease voltage difference, connect minus lead of voltmeter to GND test point of Regulator/Audio PCB and plus lead to GND test point of game PCB. Note the voltage. Now connect minus lead of voltmeter to +5 REG test point on Regulator/Audio PCB and plus lead to +5 test point on game PCB. From this you can see which harness circuit is dropping the voltage. Troubleshoot the appropriate harness wire or harness connector.

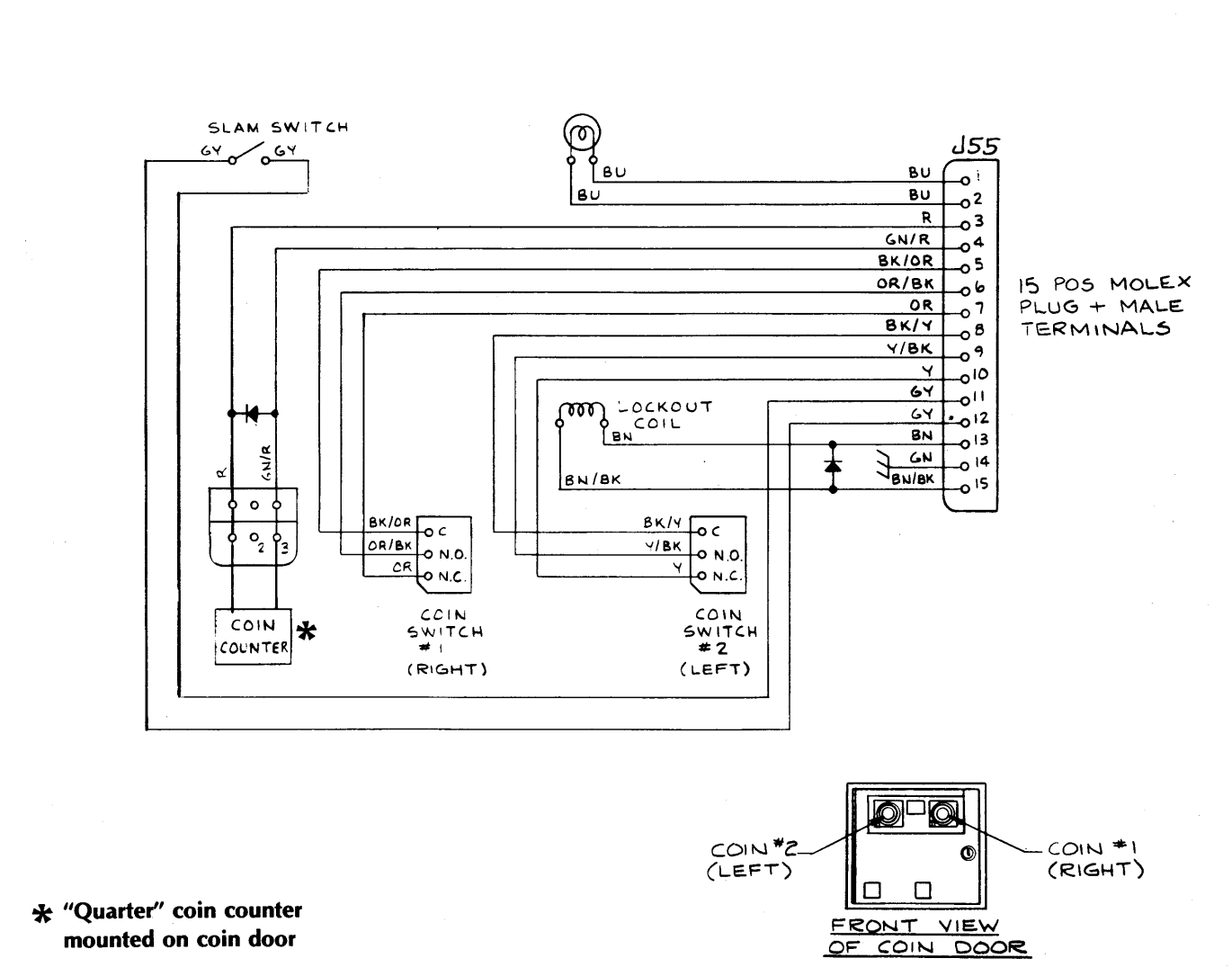
Audio Circuit

The audio circuit contains two independent audio amplifiers. Each amplifier consists of a TDA2002AV amplifier with a gain of ten. The AUDIO DISABLE input from the game PCB inhibits both amplifiers from generating any audio during the attract mode.

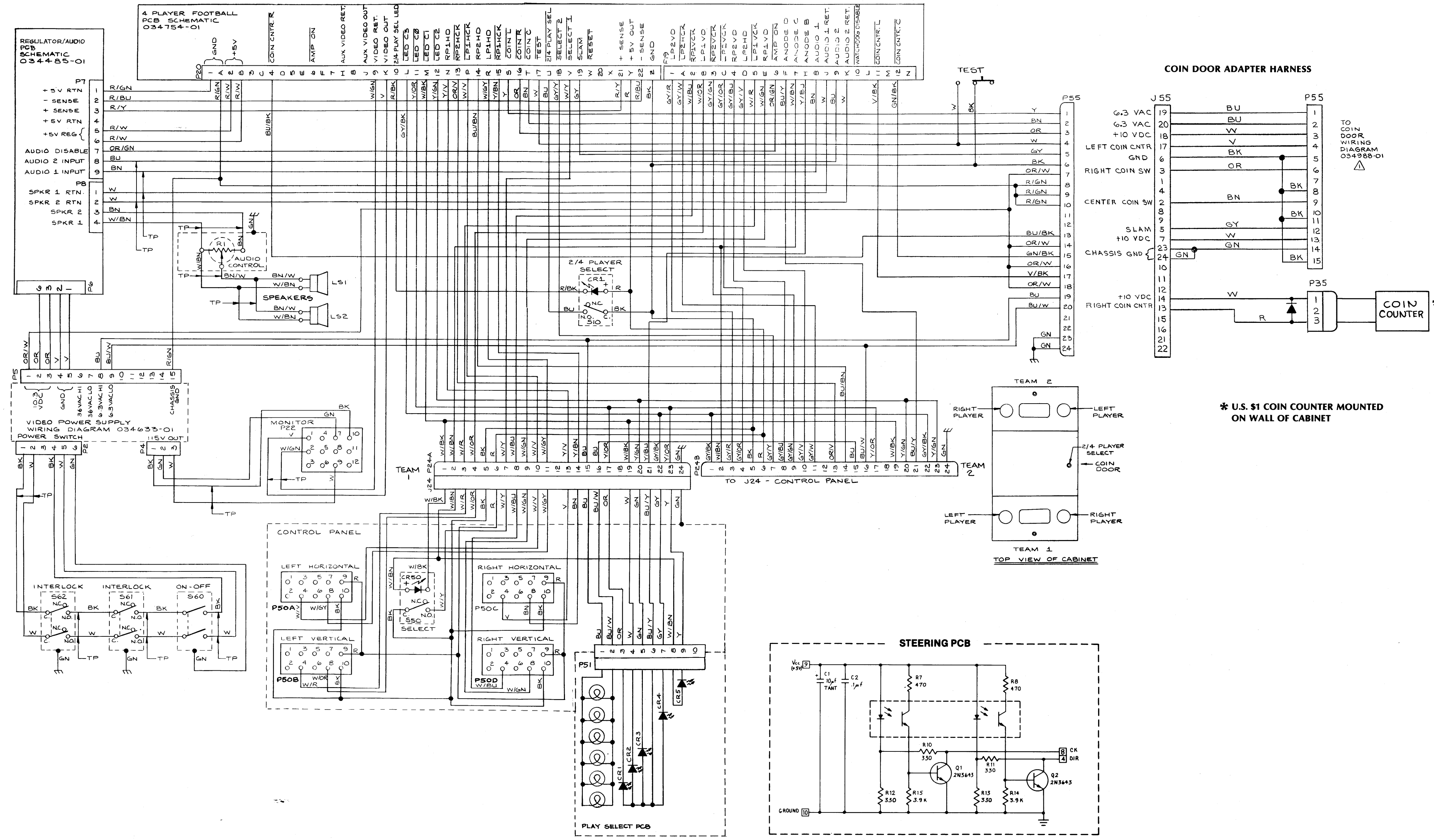
The audio circuit is repeated on Sheet 1, Side B including more information about its operation.



COIN DOOR SCHEMATIC (030401-01 B)



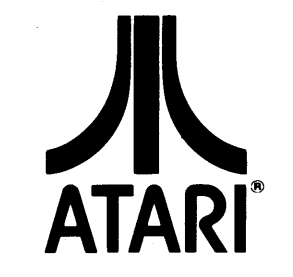
GAME WIRING DIAGRAM



Drawing Package Supplement
to
4-PLAYER FOOTBALL™
Operation, Maintenance, and Service Manual

Contents of this Drawing Package

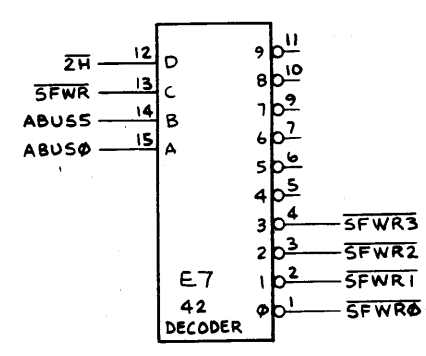
- Game Wiring Diagram
 - Microcomputer, Clock, Sync and Memory
 - Video Generator and Alphanumeric Generator
 - Switch Inputs, Audio, Coin Counter and LED Outputs
- Sheet 1, Side A
Sheet 1, Side B
Sheet 2, Side A
Sheet 2, Side B



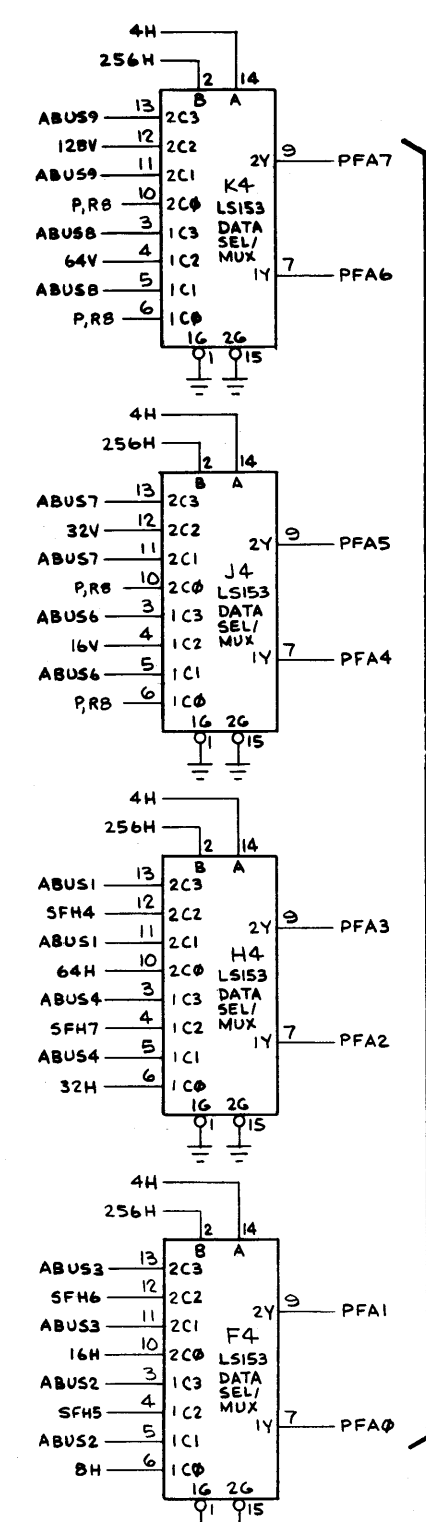
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VIDEO GENERATOR

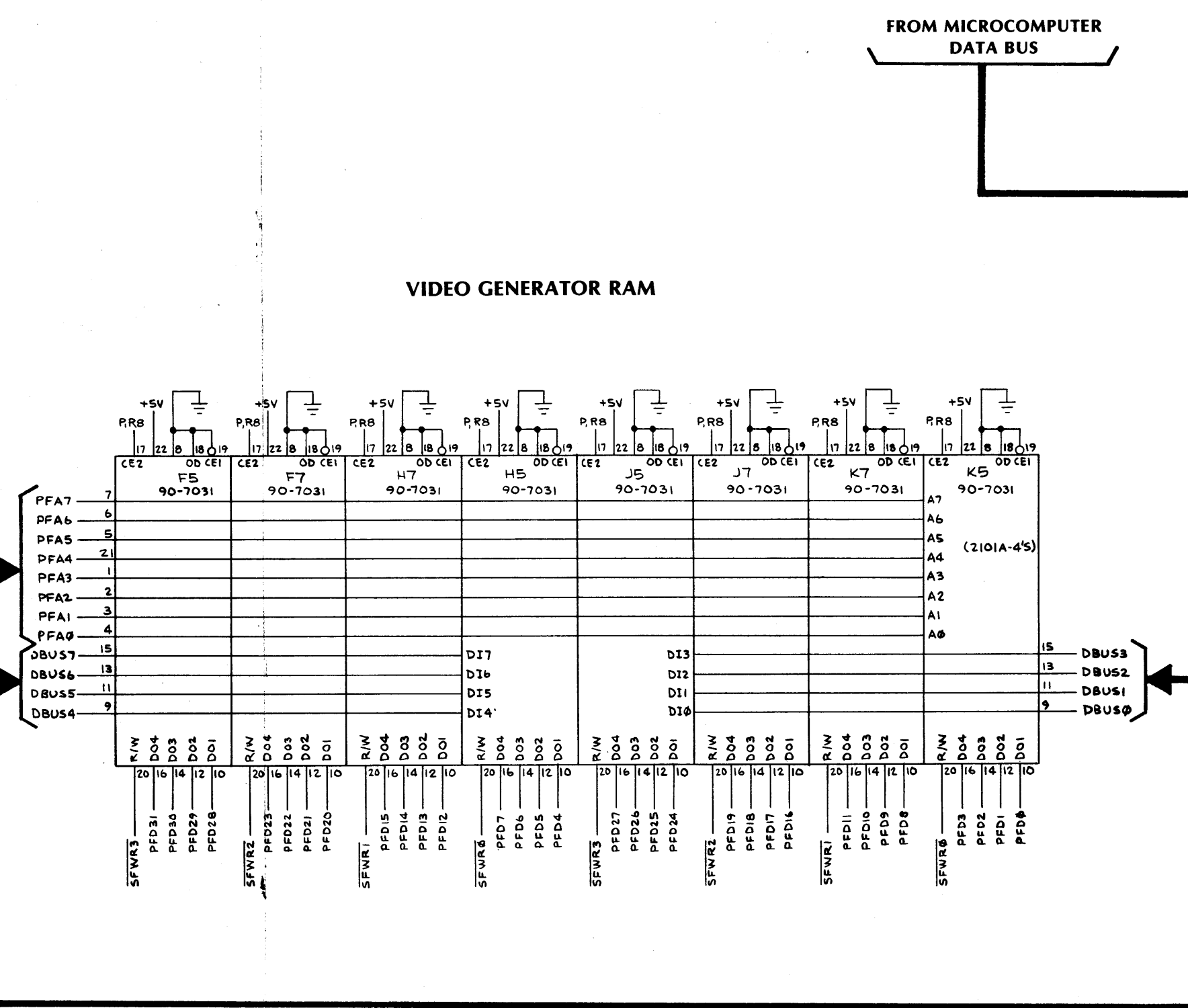
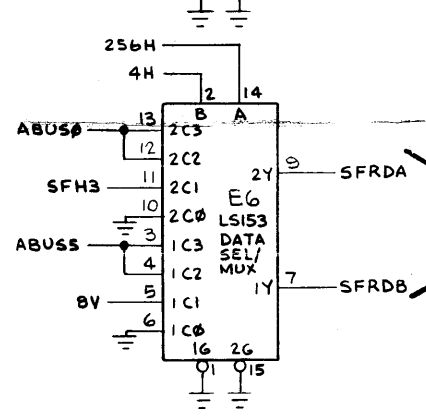
The address decoder outputs the scrollfield write enable signal SFWR, and the microprocessor selects the appropriate RAM pair with address lines ABUS0 and ABUS5.



Data Selectors F4, H4, J4 and K4 select the addressing mode for the Video Generator RAM. When 4H is high, the MPU addresses the RAM, via ABUS 0-9. When 4H is low, the Video Generator RAM is addressed by either the scrollfield horizontal address (SFH 3-7) or by the sync chain (8H-64H and 16V-128V). 256H determines which of these two addresses the RAM when 4H is low. When 256H is low sync is selected. When 256H is high, scrollfield is selected.

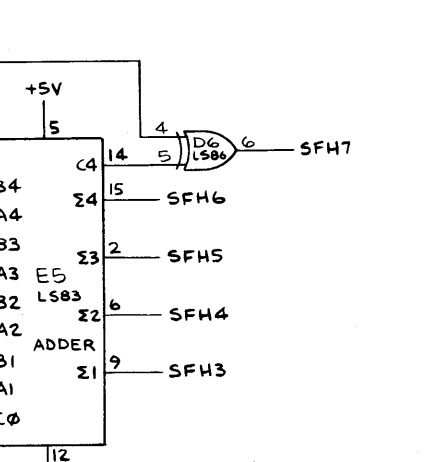


Multiplexer E6 selects the output of the RAM.



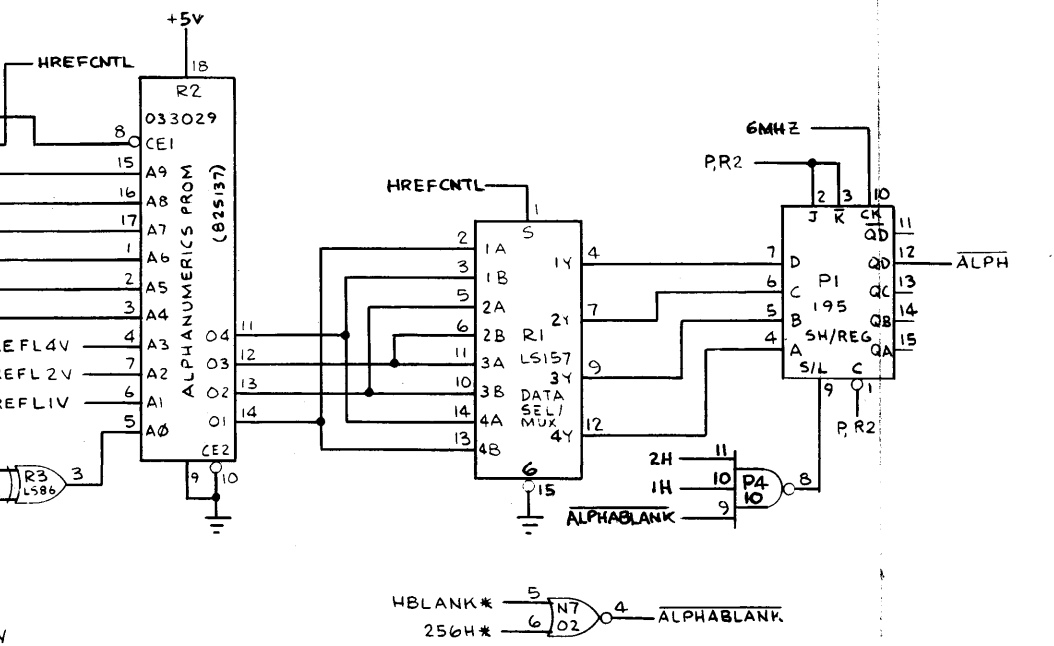
When the RAM is written to by the microprocessor, SFWR is low and a RAM pair is written to by the selection of ABUS0 and ABUS5. Data is written into the RAM through data bus DBUS0 thru DBUS7. Data is read out of the RAM on data lines PFD0 thru PFD31.

The latched data output of D5 is compared with horizontal sync 8H thru 64H, to enable the playfield to scroll (shift) in steps of 8H. SFH0 thru SFH7 selects the scrollfield output from multiplexer C8 in steps of 1H.

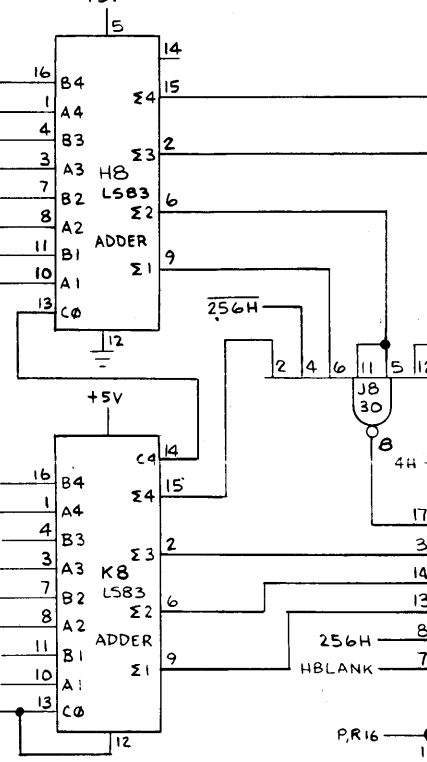
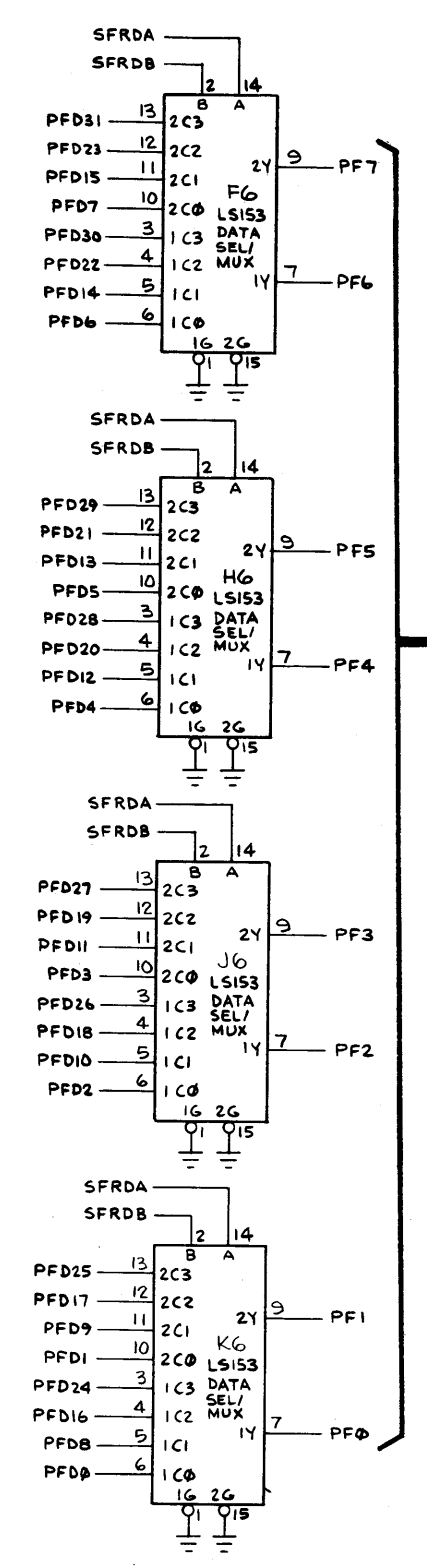


ALPHANUMERICS GENERATOR

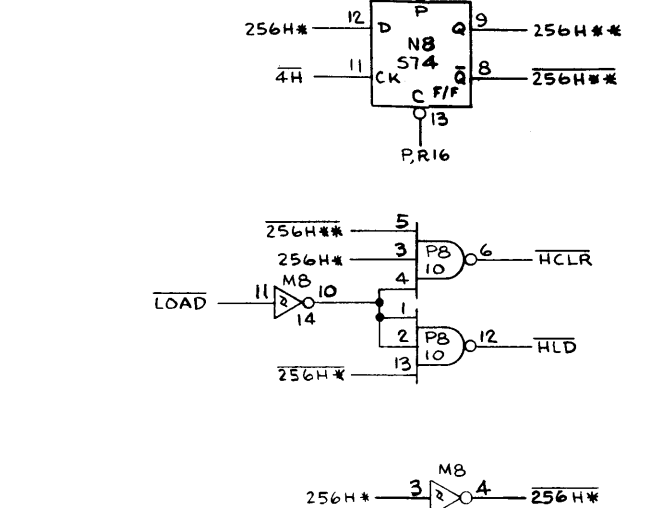
Alphanumerics data is stored in the microcomputer RAM. This information is latched at the output of latch P2 when the microprocessor reads the RAM. Latched RAM data RAMD0 thru RAMD5 addresses the alphanumerics PROM R2. The RAMD7 signal enables the PROM. RAMD6 is used to invert (reflect) the data output of the PROM both horizontally and vertically at the output of multiplexer R1. Therefore, the same data output is used at both ends of the monitor. The ALPHABLANK signal ensures that the alphanumerics appear only at each end of the horizontal scan line.



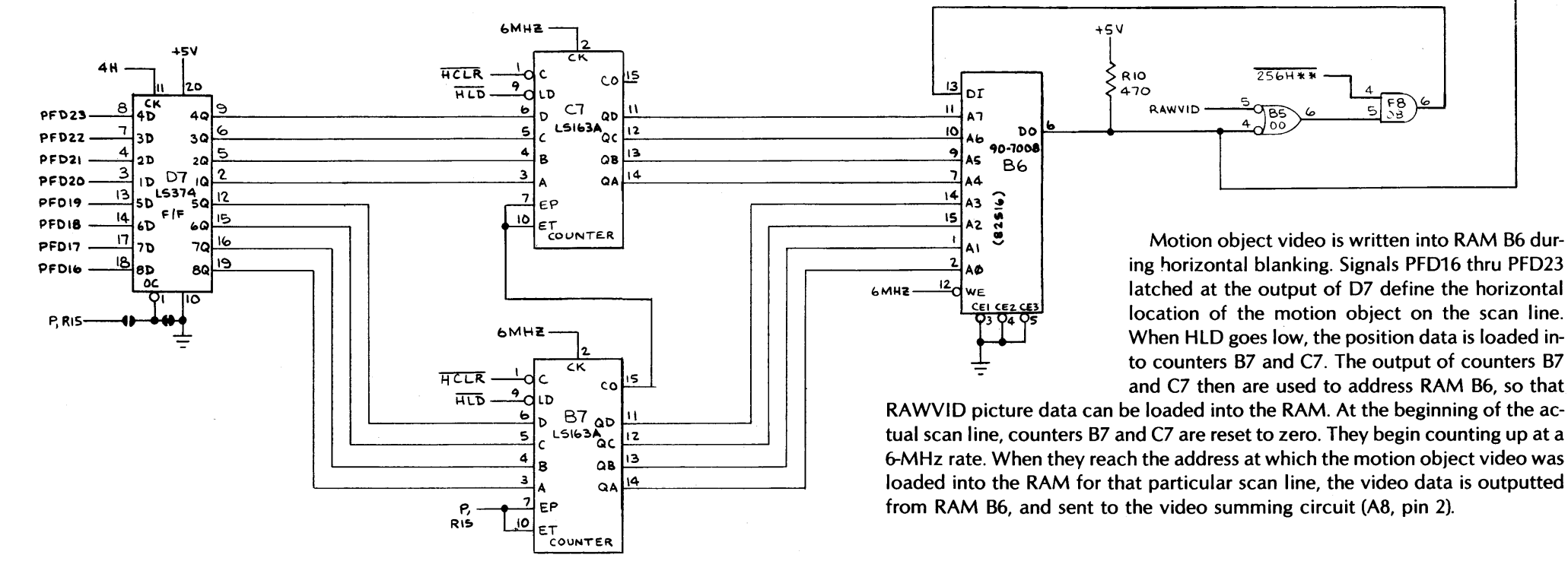
FROM MICROCOMPUTER DATA BUS



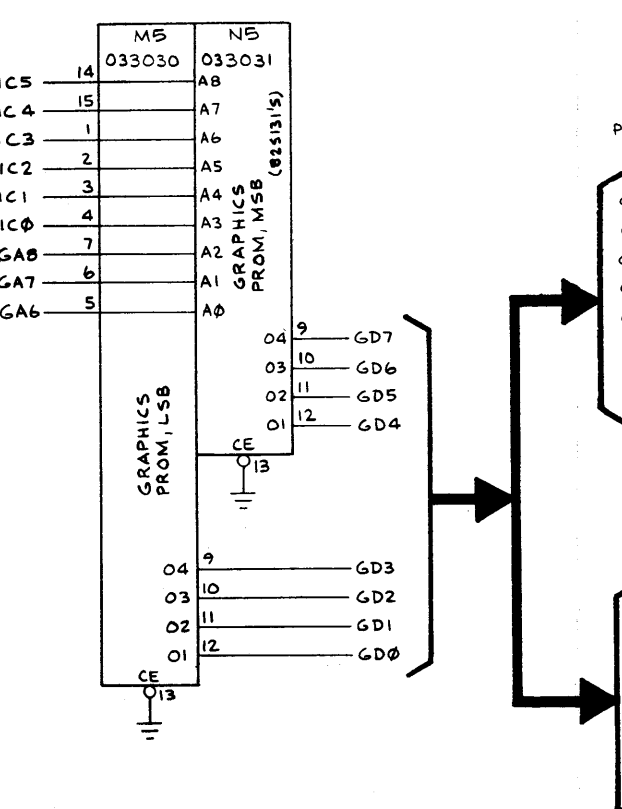
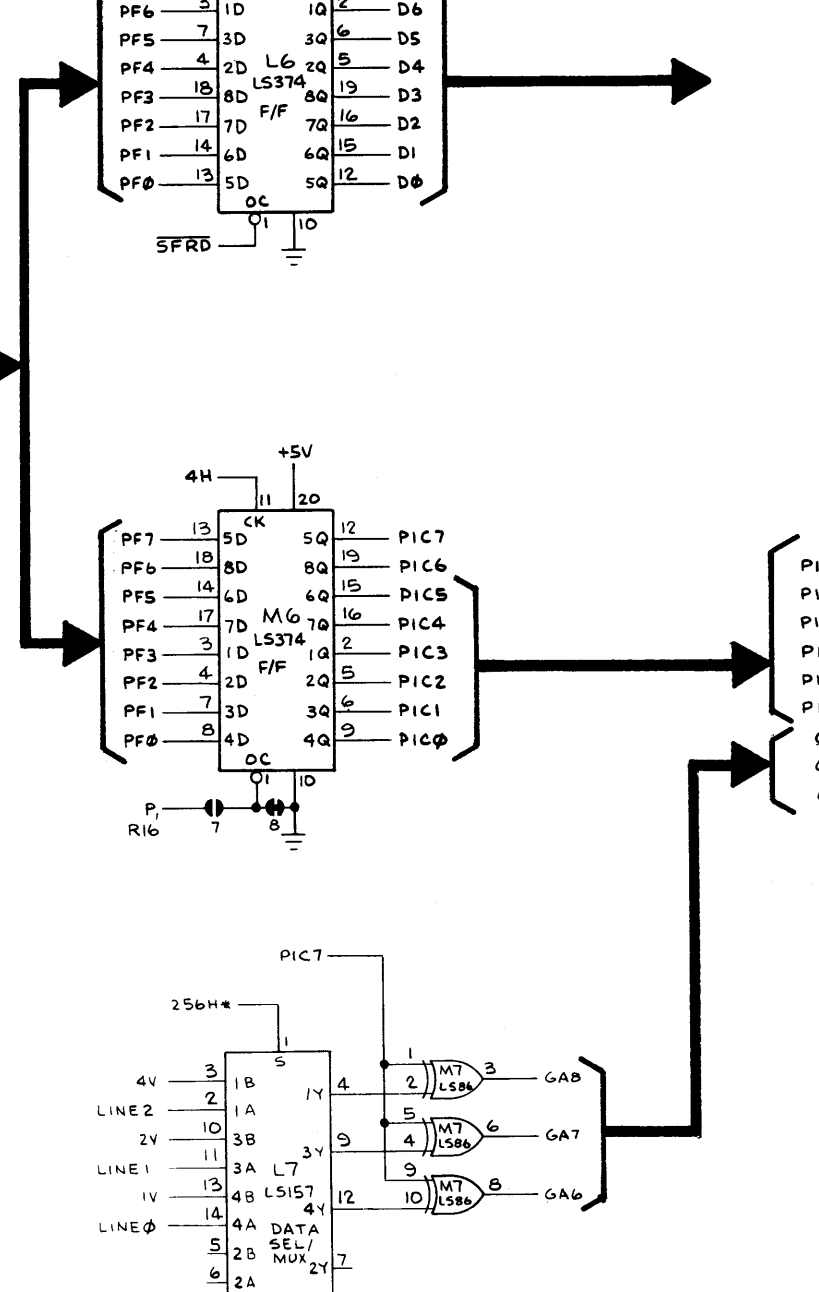
Addresses H8 and K8 compare the vertical line presently scanned with RAM data PFD0 thru PFD15, which define the vertical location of the motion object. When the inputs are equal, MATCH is latched low, permitting the motion object data to be output from the graphics PROM. LINE0 thru LINE7 count up for the eight scan lines of the motion object picture.



Motion object video is written into RAM B6 during horizontal blanking. Signals PFD16 thru PFD23 latched at the output of D7 define the horizontal location of the motion object on the scan line. When HLD goes low, the position data is loaded into counters B7 and C7. The output of counters B7 and C7 then are used to address RAM B6, so that the RAWVID picture data can be loaded into the RAM. At the beginning of the actual scan line, counters B7 and C7 are reset to zero. They begin counting up at a 6-MHz rate. When they reach the address at which the motion object video was loaded into the RAM for that particular scan line, the video data is outputted from RAM B6, and sent to the video summing circuit (A8, pin 2).

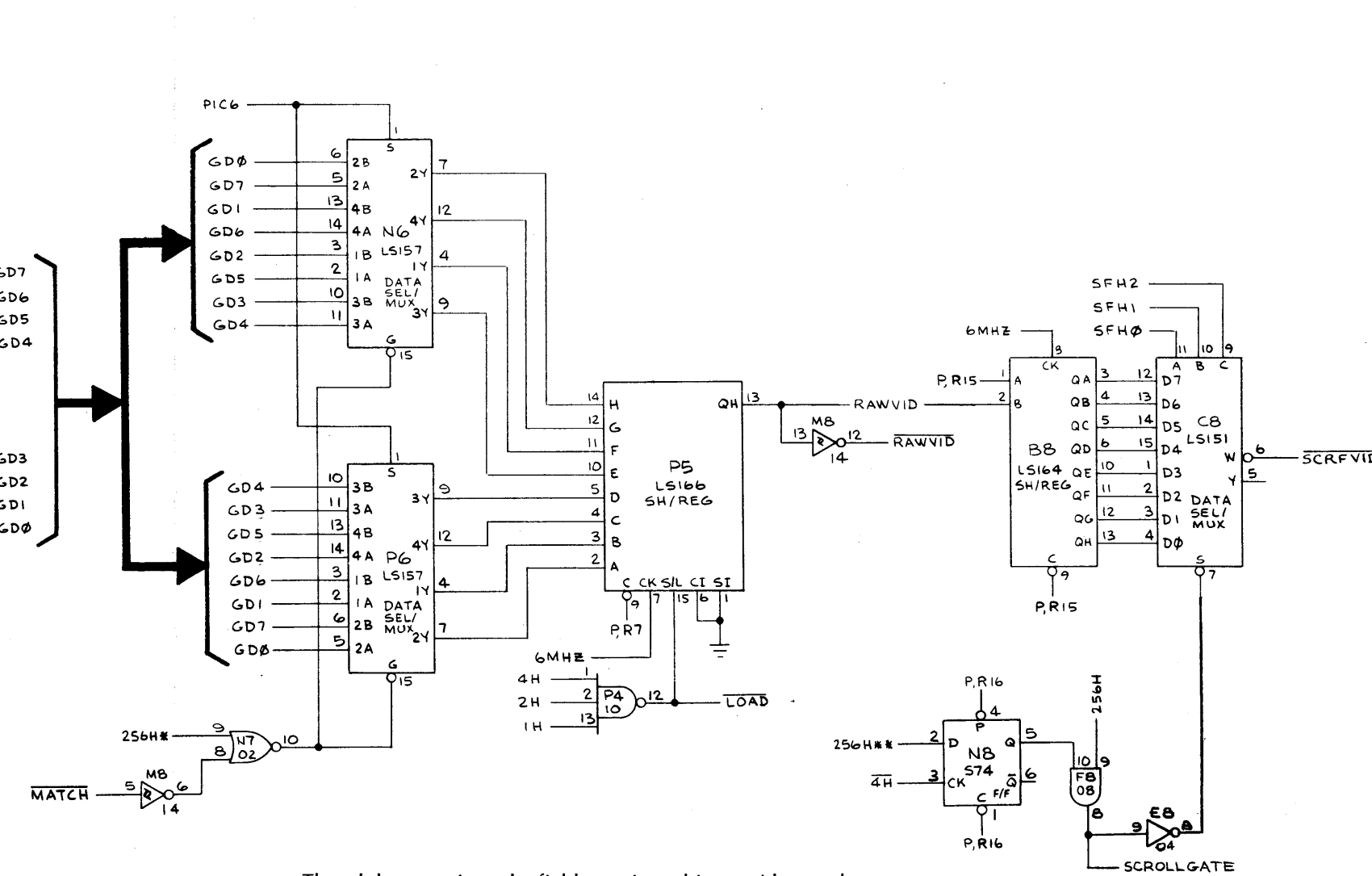


The microprocessor reads the latched playfield and motion objects data bytes on data lines D0 thru D7.

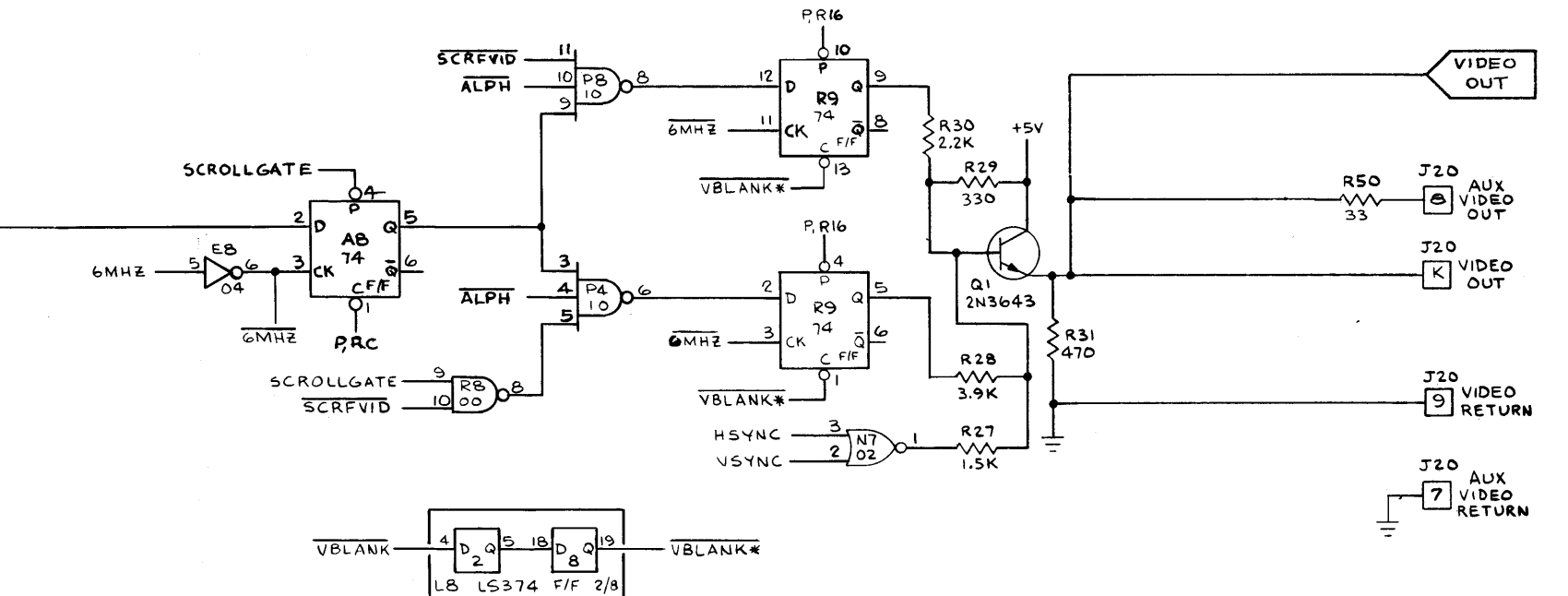


Graphics PROMs M5 and N5 contain the graphics data for both the playfield and motion objects. Address inputs PIC0 thru PIC5 select the picture. Inputs GA6 thru GA8 select the actual line of the picture to be output. PIC7 determines whether or not the picture is reflected vertically. PIC6 determines whether or not the picture is reflected horizontally. When MATCH is low, the multiplexers are enabled for writing motion object video data into motion object RAM B6.

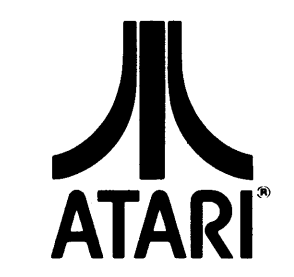
The alphanumerics, playfield, motion objects video and vertical and horizontal sync signals are all summed at the video summer. The VBLANK signal ensures that there is no video during the vertical blanking period.



The SCROLLGATE signal ensures that the playfield and motion object video is only output during the portion of the screen scanned, when 256H is high, conditioned by 256H**.

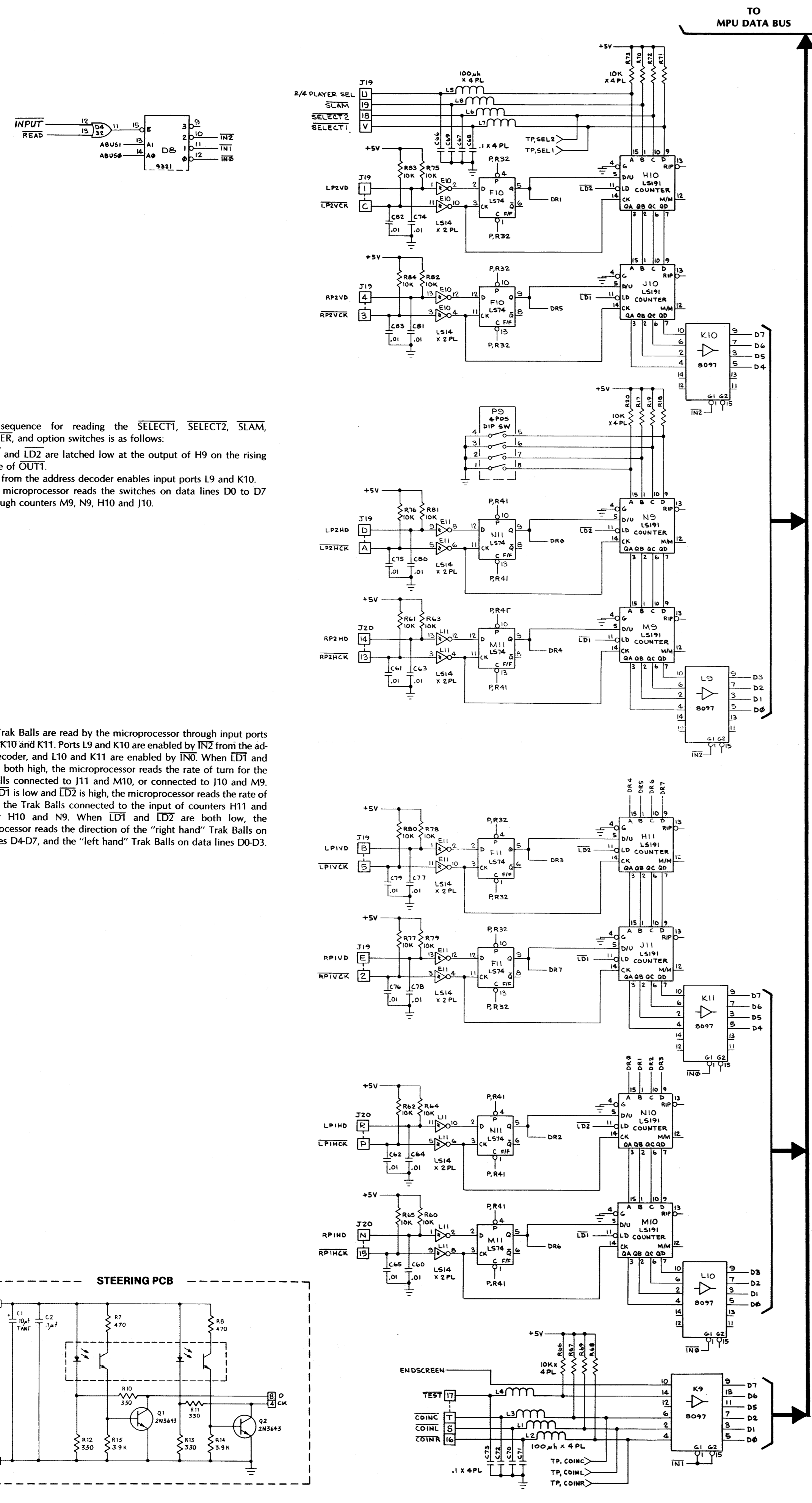


denotes a test point



4-PLAYER FOOTBALL VIDEO GENERATOR AND ALPHANUMERICS GENERATOR 034754-xx A

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The sequence for reading the SELECT1, SELECT2, SLAM, 2/4PLAYER, and option switches is as follows:

- LD1 and LD2 are latched low at the output of H9 on the rising edge of OUT1.
- IN2 from the address decoder enables input ports L9 and K10.
- The microprocessor reads the switches on data lines D0 to D7 through counters M9, N9, H10 and J10.

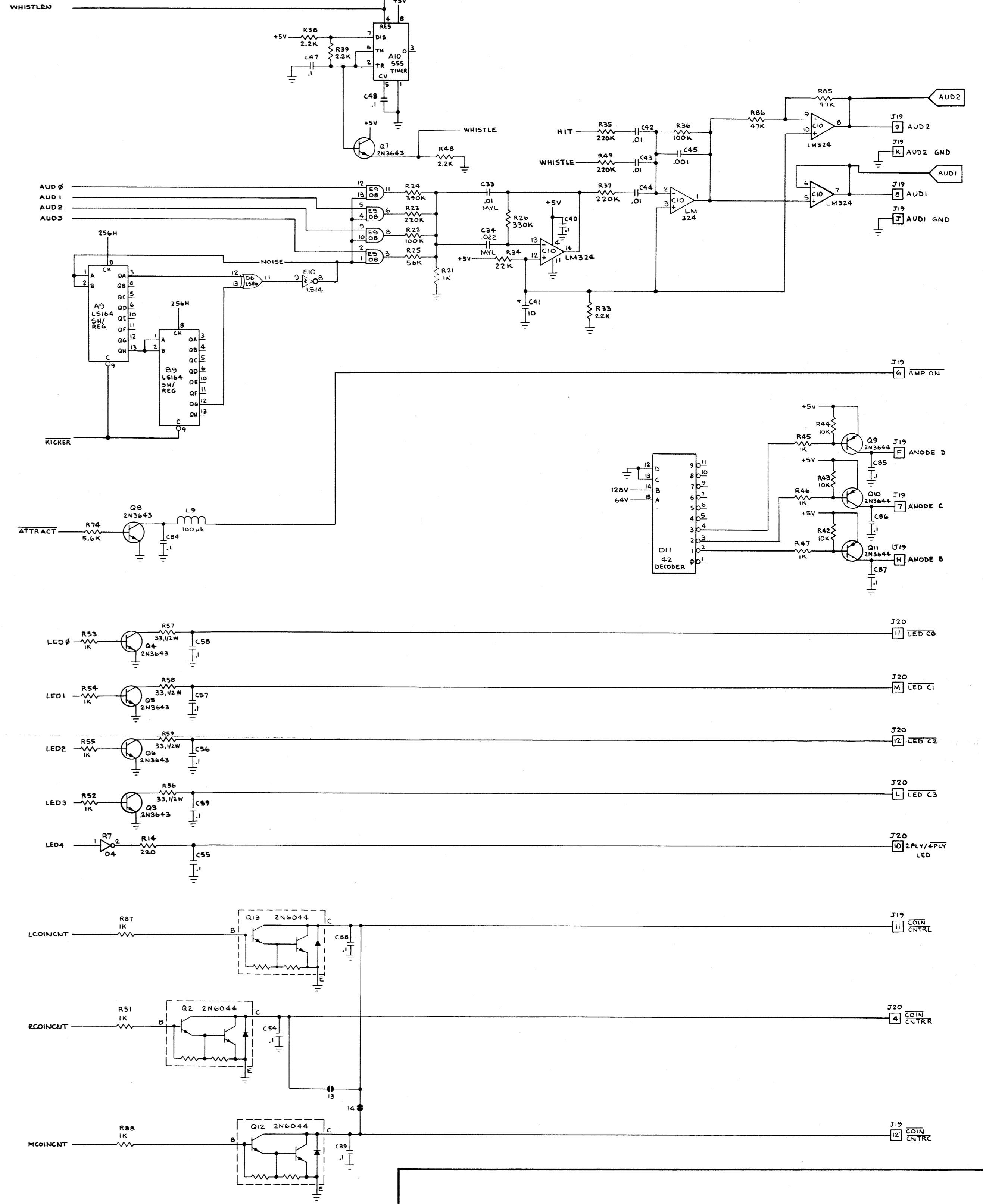
The Trak Balls are read by the microprocessor through input ports L9, L10, K10 and K11. Ports L9 and K10 are enabled by IN2 from the address decoder, and L10 and K11 are enabled by IN0. When LD1 and LD2 are both high, the microprocessor reads the rate of turn for the Trak Balls connected to J11 and M10, or connected to J10 and M9. When LD1 is low and LD2 is high, the microprocessor reads the rate of turn for the Trak Balls connected to the input of counters H11 and N10, or H10 and N9. When LD1 and LD2 are both low, the microprocessor reads the direction of the "right hand" Trak Balls on data lines D4-D7, and the "left hand" Trak Balls on data lines D0-D3.

The audio generator generates the crowd, hit, and whistle sounds. The crowd sound is generated from random noise from A9 and B9. The volume of the crowd sound is controlled the AUD0 thru AUD3 data latched at the output of F9. Hit is enabled by the HIT data latched at the output of H9. A "hit" occurs when the ball is caught or kicked.)

Whistle is enabled by WHISTLEN data from the output of latch H9. The audio output to the Regulator/Audio PCB is out of phase at the J19 connector, pins 8 and 9. Therefore, the audio section of the Regulator/Audio PCB acts as a push-pull amplifier. The amplifier is enabled when ATTRACT, from latch F9, is high.

The LEDs on the top of the 4-Player Football game are connected in a matrix. The anodes are strobed by vertical sync. The cathodes are controlled by latched data from the microcomputer. The LEDCL signal is generated by the IRQ counter at the IRQ input of the microprocessor. Since the microprocessor knows when each LED anode driver is being strobed at any given time, all the microprocessor needs to do to light an LED is latch the appropriate data line by outputting the address for the OUT3 enabling signal from the address decoder. When the latched data line is high, the appropriate LED is lighted. Team 1 LEDs, excluding their kick LED, are connected to anode B. All Team 2 LEDs, excluding their kick LED, are connected to anode D. The kick LEDs of both Team 1 and Team 2 are connected to anode C.

Coin and self-test switch inputs are connected to +5 VDC through pullup resistors. When a switch is closed, that input is pulled to ground. The switch is read by the microprocessor when switch input port K9 is enabled by INT from the address decoder.



denotes a test point

4-PLAYER FOOTBALL SWITCH INPUTS, COIN COUNTER AND LED OUTPUTS 034754-xx A



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