

Schematic Package Supplement to

ATARI SYSTEM I™

Operators Manual

NOTE

This staple temporarily holds the schematic package together. Remove the staple before using these schematics.



 A Warner Communications Company

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SYSTEM I MAIN PCB
SCHEM SEE SHTS. 5A-
9B

1 + SENSE
2 +5V
3 +10.3V RESET
4 - SENSE
5 -15V
6 RTN
7 +15V
8 +5V
9 +5V
10 +5V
11 RTN
12

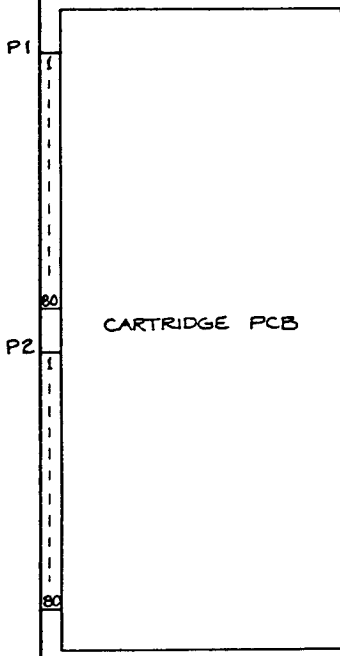
Y
2 R
3 OR
4 BK
5 GY
6 BN
7 Y
8 R
9 R
10 R
11 BN
12

SEE SPECIFIC GAME KIT FOR CONTROL WIRING DIAGRAM

J106
1 +5V
2 N/C
3 LED 2
4 LED 1
5 KEY
6 SW 5
7 SW 2
8 SW 4
9 SW 1
10 SW 3
11 GND

J102
1 +5V
2 UP 2/VERT. 4
3 DN 2/HORZ 4
4 LT 2/VERT 3
5 RT 1/HORZ 1
6 RT 2/HORZ 3
7 LT 1/VERT 1
8 UP 1/VERT 2
9 DN 1/HORZ 2
10 KEY
11 GND

J103
1 +5V
2 HORZ CLK 2
3 HORZ DIR 2
4 VERT CLK 2
5 VERT DIR 2
6 HORZ CLK 1
7 HORZ DIR 1
8 VERT CLK 1
9 KEY
10 VERT DIR 1
11 GND



+ SENSE
+5V
+10.3V UNREG
- SENSE
-15V
RTN
+15V
+5V
+5V
RTN

F7

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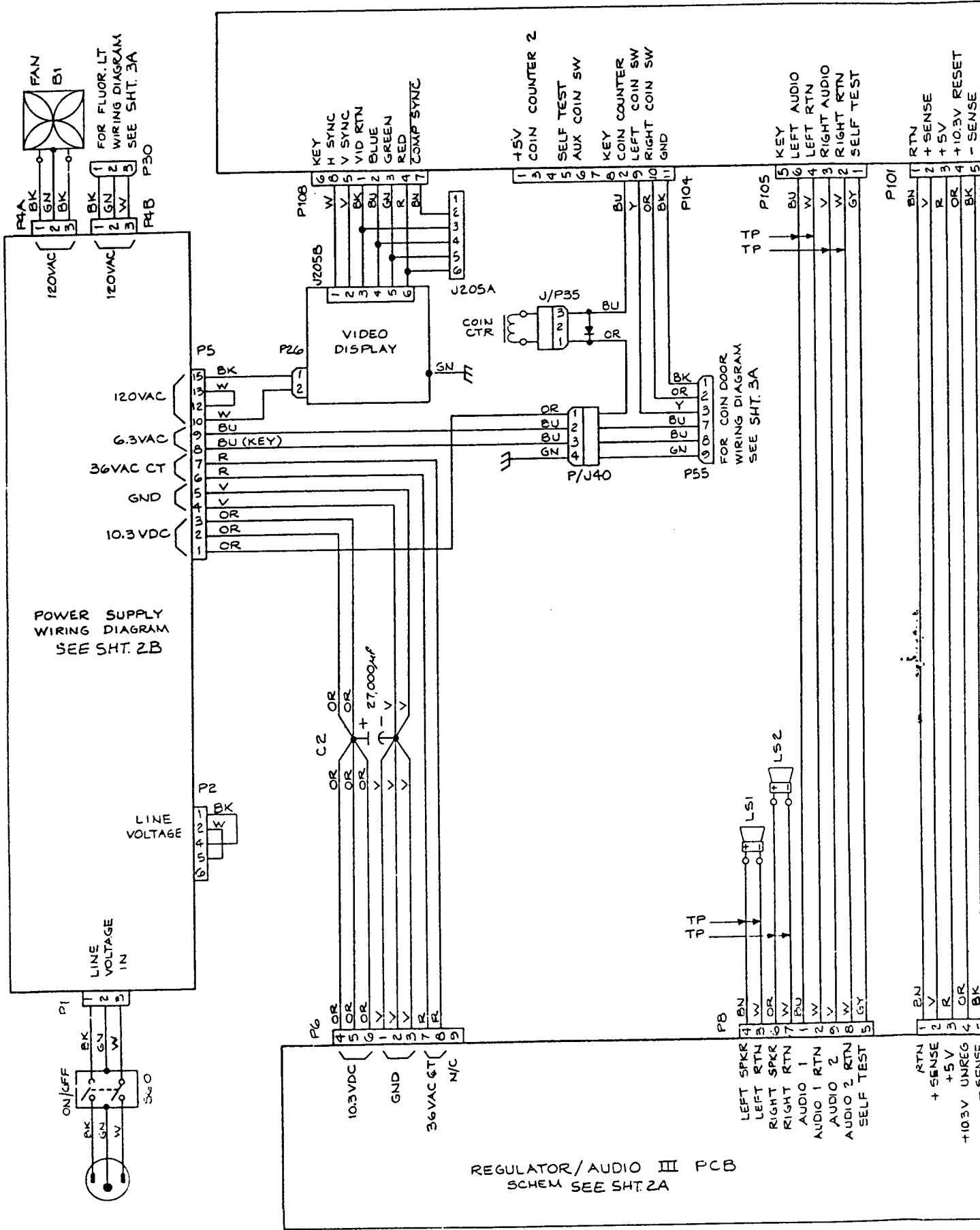
System I™ Main Wiring Diagram



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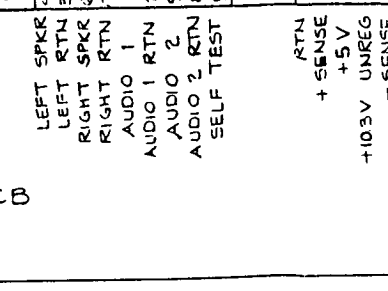
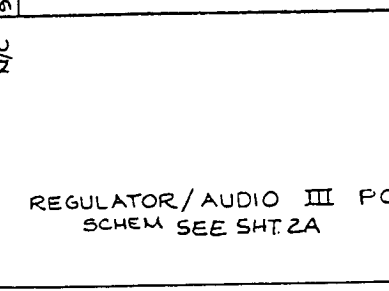
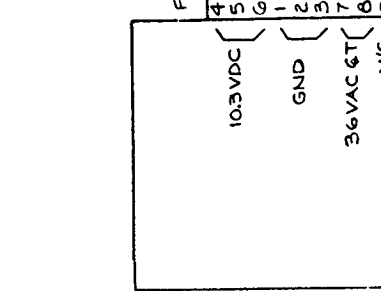
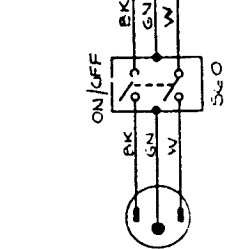
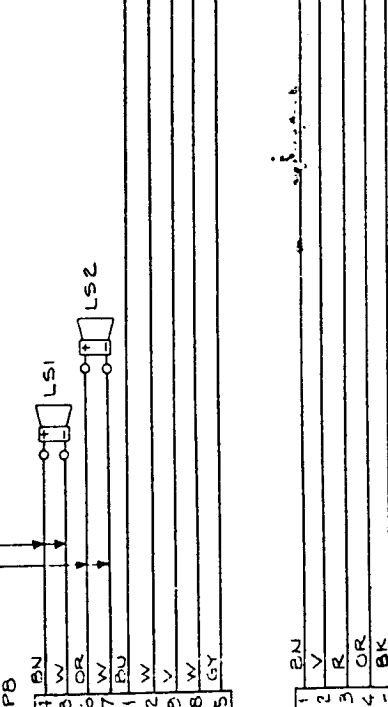
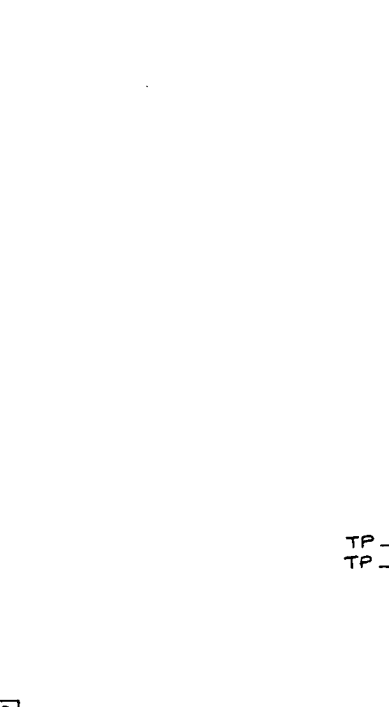
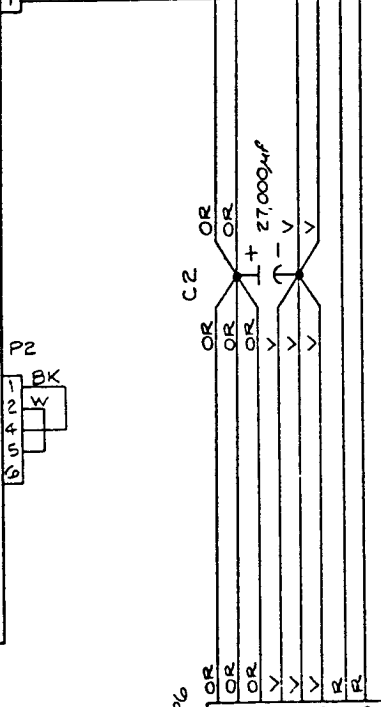
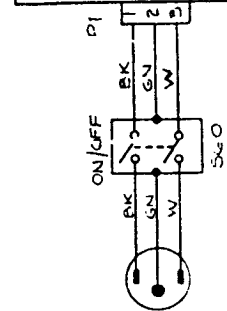
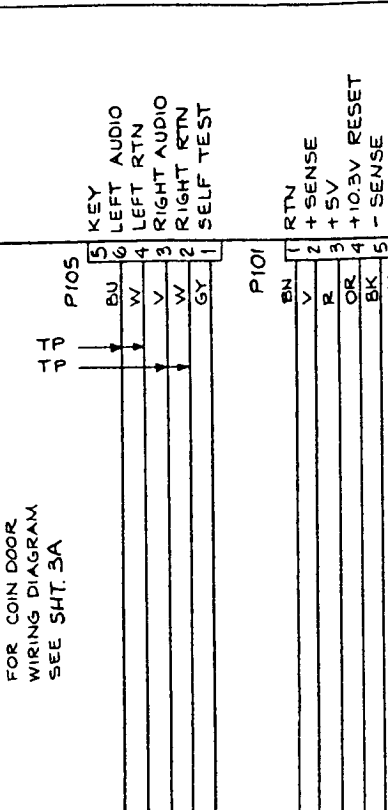
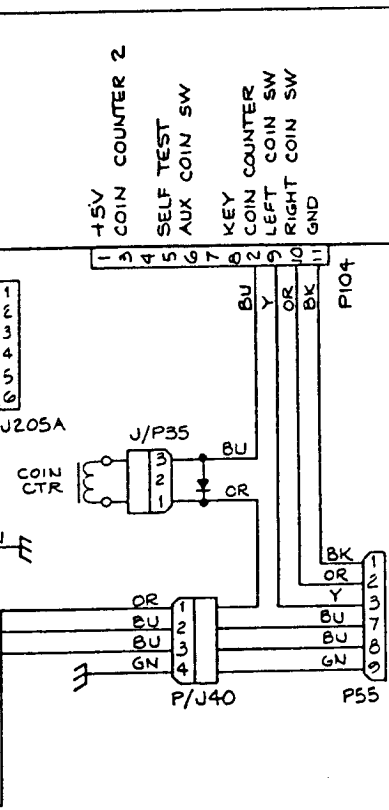
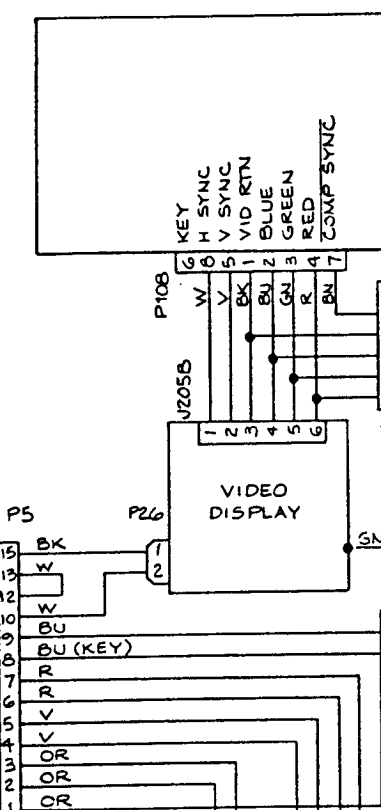
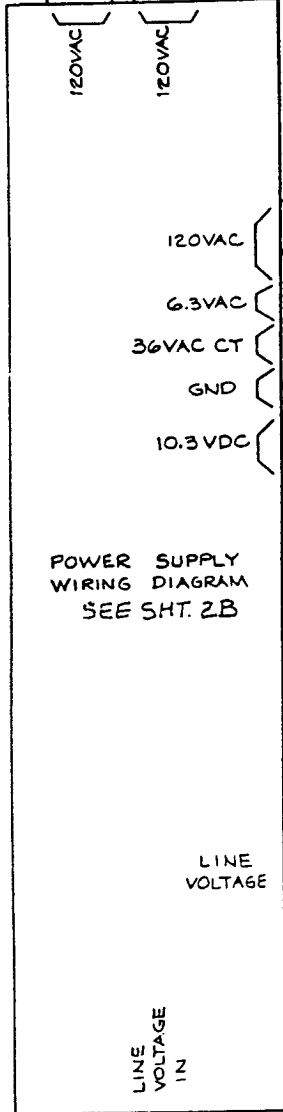
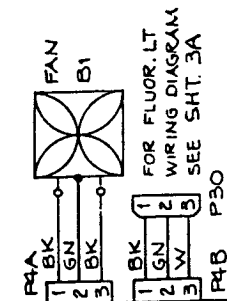
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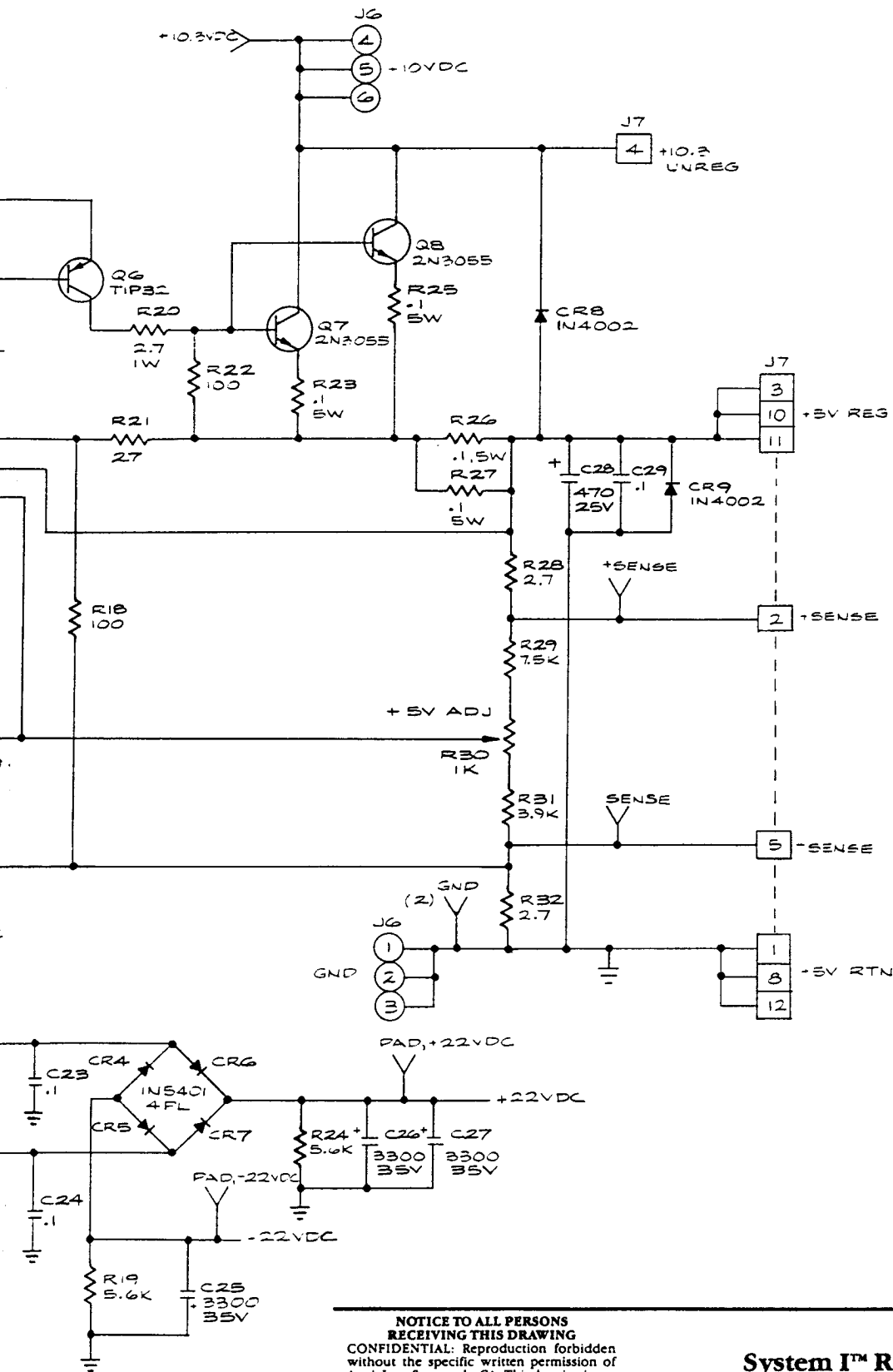
SP-277 Sheet 1B
1st printing



POWER SUPPLY
WIRING
DIAGRAM
SEE SHT. 2B

REGULATOR/AUDIO III PCB
SCHEM SEE SHT. 2A

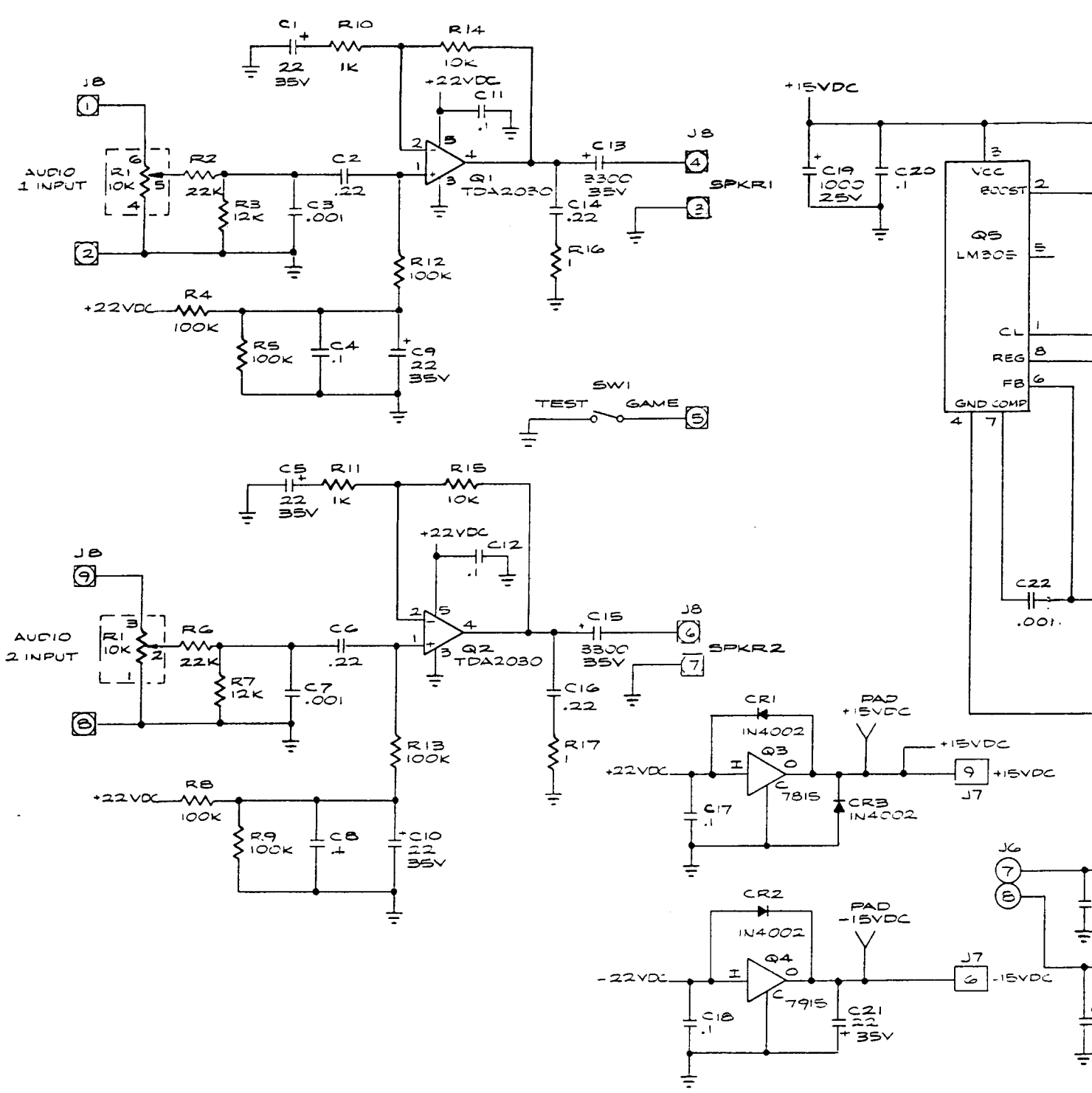


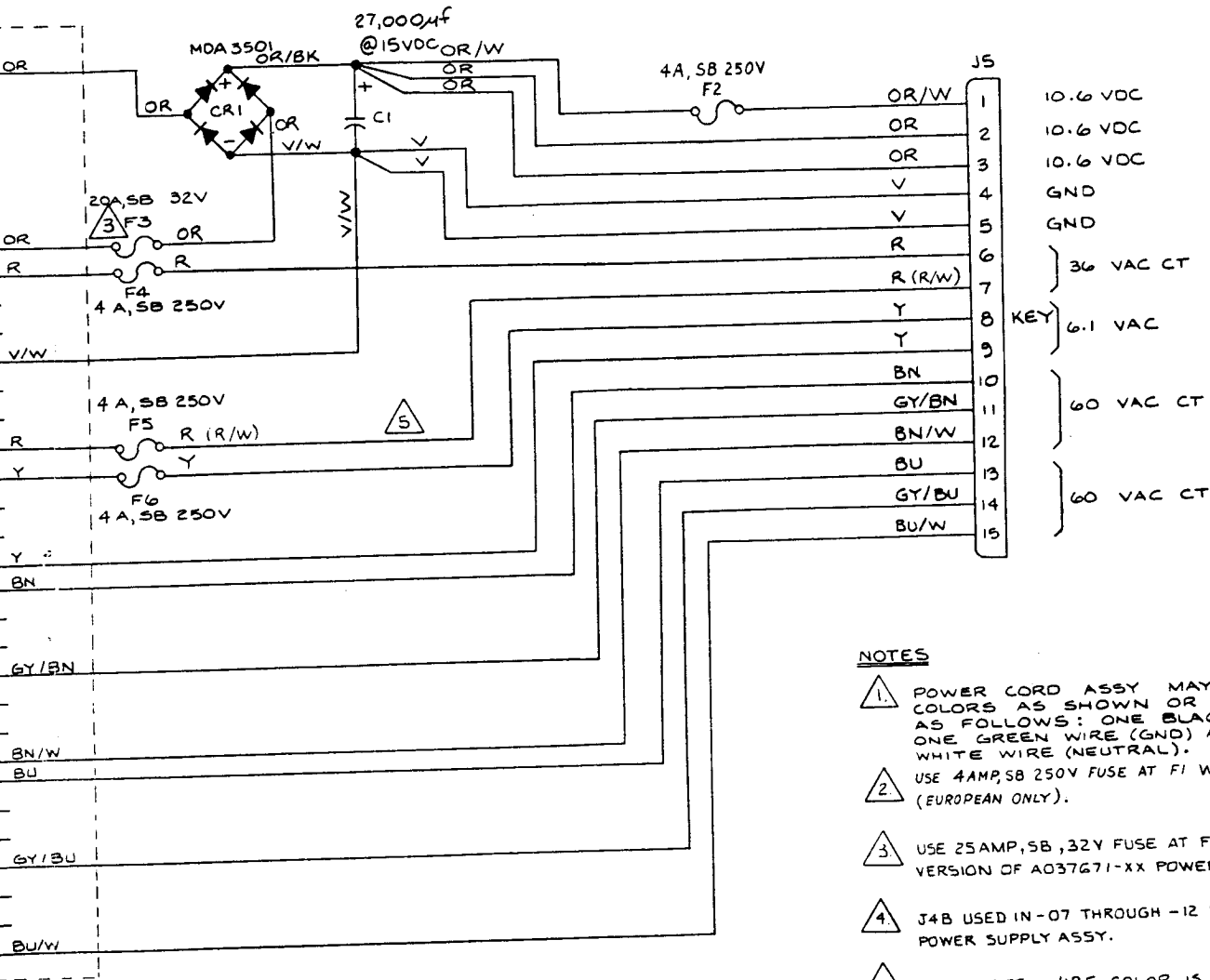


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System I™ Regulator/Audio III PCB Schematic Diagram







NOTES

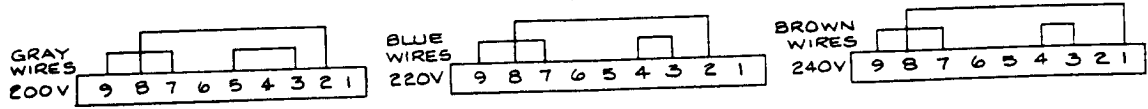
- 1. POWER CORD ASSY MAY HAVE WIRE COLORS AS SHOWN OR WIRE COLORS AS FOLLOWS: ONE BLACK WIRE (AC), ONE GREEN WIRE (GND) AND ONE WHITE WIRE (NEUTRAL).
- 2. USE 4AMP, SB 250V FUSE AT F1 WITH 220V & 240V (EUROPEAN ONLY).
- 3. USE 25AMP, SB, 32V FUSE AT F3 FOR -04, -05, & -06 VERSION OF A037671-XX POWER SUPPLY.
- 4. J4B USED IN -07 THROUGH -12 VERSION OF A037671-XX POWER SUPPLY ASSY.
- 5. ALTERNATE WIRE COLOR IS IN PARENTHESES ().

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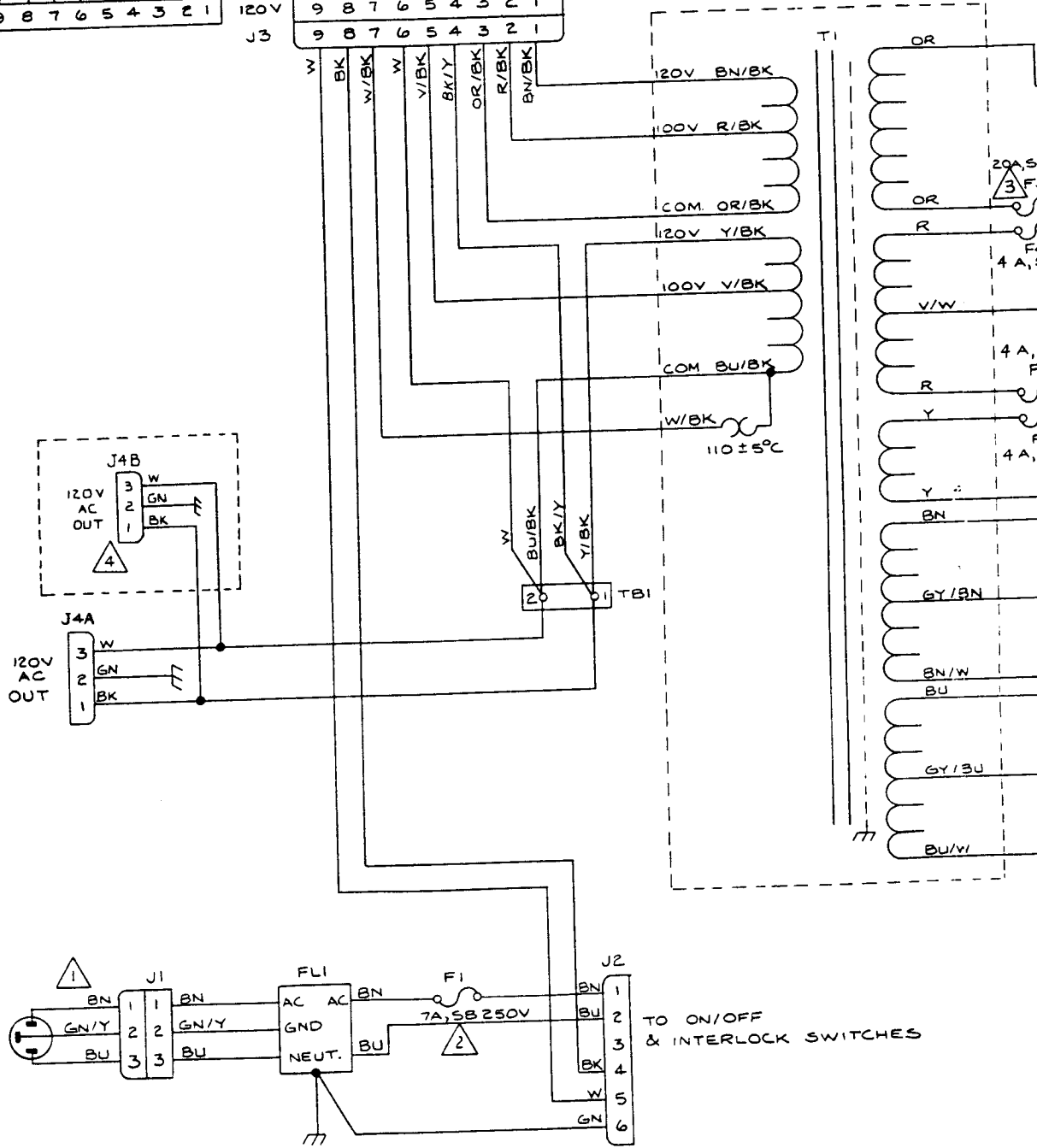
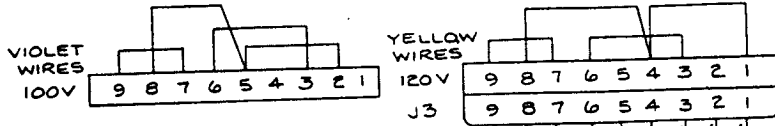
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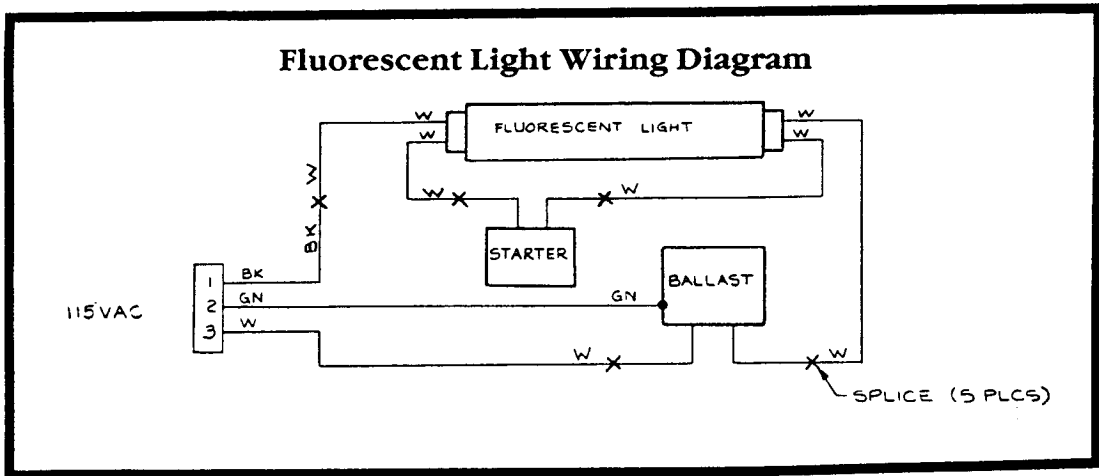
System I™ Color Raster Power Supply Wiring Diagram





VOLTAGE SELECTION BLOCKS





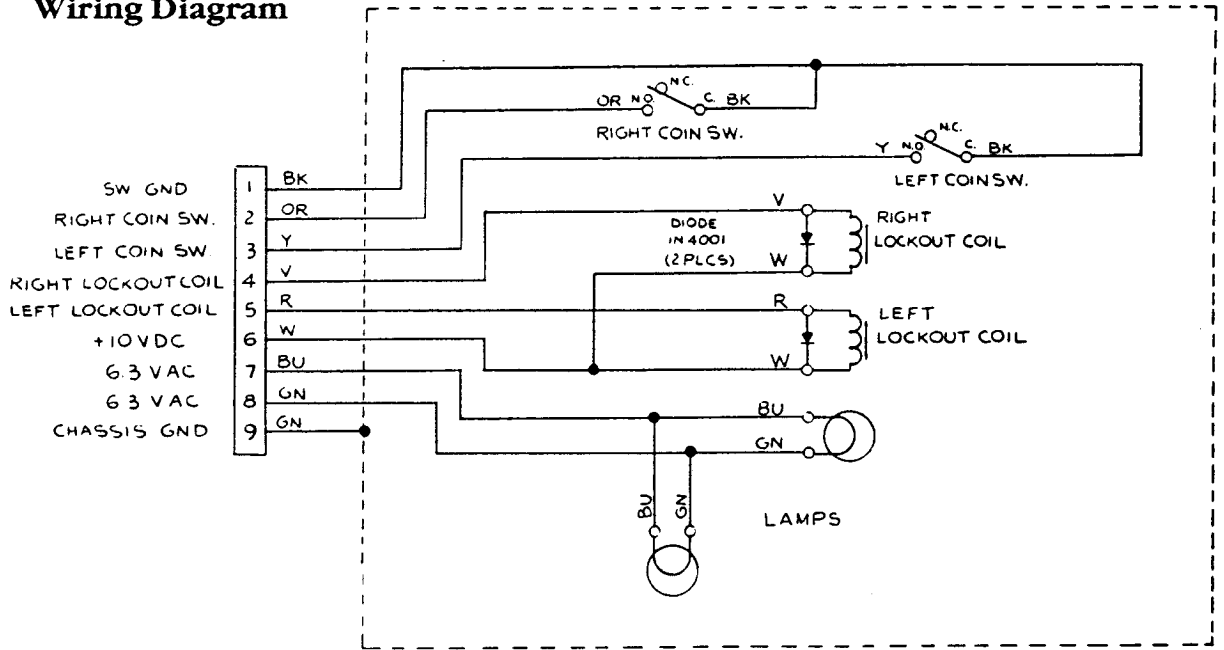
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System I™ Game Interfaces



Coin Door Wiring Diagram



Processor Memory Map

ADDRESS LINES											DATA BUS SIGNAL LINES																
A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	READ/ WRITE	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
A	A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	0	0	0	0	0	0	0	0	0	W							D	D	D	D	D	D	D	D	D	D
0	0	0	0	0	0	0	0	0	0	0	W							D	D	D	D	D	D	D	D	D	D
0	0	0	0	0	0	0	0	0	0	0	R								D	D	D	D	D	D	D	D	D
0	0	0	0	0	0	0	0	0	0	0	W								D								
0	0	0	0	0	0	0	0	0	0	0	W									D							
0	0	0	0	0	0	0	0	0	0	0	W										D						
0	0	0	0	0	0	0	0	0	0	0	W											D					
0	0	0	0	0	0	0	0	0	0	0	W												D				
0	0	0	0	0	0	0	0	0	0	0	W													D			
0	0	0	0	0	0	0	0	0	0	0	W														D		
0	0	0	0	0	0	0	0	0	0	0	W															D	
0	0	0	0	0	0	0	0	0	0	0	W																D
A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	0	0	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	0	1	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	1	0	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	1	1	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	0	0	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	0	1	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	0	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	1	1	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
1	1	0	0	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
1	1	0	1	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
1	1	1	0	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
1	1	1	1	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
A	A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	0	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
0	1	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
1	0	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
1	1	0	0	0	0	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
A	A	A	A	A	A	A	A	A	A	A	R									D	D	D	D	D	D	D	D
0	0	0	0	0	0	0	0	A	A	A	R									D	D	D	D	D	D	D	D
0	0	0	0	0	0	0	0	A	A	A	R									D	D	D	D	D	D	D	D
0	0	0	0	0	0	1	0	0	0	0	R																
0	0	0	0	0	0	0	0	0	0	0	R									D							
0	0	0	0	0	0	0	0	0	0	0	R										D						
0	0	0	0	0	0	0	0	0	0	0	R											D					
0	0	0	0	0	0	0	0	0	0	0	R												D				
0	0	0	0	0	0	0	0	0	0	0	R													D			
0	0	0	0	0	0	0	0	0	0	0	R														D		
0	0	0	0	0	0	0	0	0	0	0	R															D	
0	0	0	0	0	0	0	0	0	0	0	R																D
0	0	0	0	0	0	0	0	0	0	0	W																D
0	0	0	0	0	0	0	0	0	0	0	W																D

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System I™ Video Microprocessor Memory Map



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Microprocessor Memory Map

BUS SIGNAL LINES										READ/ WRITE	DATA BUS SIGNAL LINES							
A9	A8	A7	A6	A5	A4	A3	A2	A1	A0		D7	D6	D5	D4	D3	D2	D1	D0
A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D
A	A	A	A	A	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D
0	0	0	0	0	0	0	0	0	A	R/W	D	D	D	D	D	D	D	D
0	0	0	0	1	0	0	0	0	0	R	D	D	D	D	D	D	D	D
0	0	0	0	1	0	0	0	0	0	W	D	D	D	D	D	D	D	D
0	0	0	1	0	0	0	0	0	0	R	D							
0	0	0	0	1	0	0	0	0	0	R				D				
0	0	0	0	1	0	0	0	0	0	R						D		
0	0	0	0	1	0	0	0	0	0	R							D	
0	0	0	0	1	0	0	0	0	0	R								D
0	0	0	1	0	0	0	0	0	0	W								D
0	0	0	1	0	0	1	0	0	0	W								D
0	0	0	1	0	0	1	0	1	0	W								D
0	0	0	1	0	0	1	1	0	0	W								D
0	0	0	1	0	0	1	1	1	0	W								D
0	0	1	1	1	A	A	A	A	A	R/W	D	D	D	D	D	D	D	D
A	A	A	A	A	A	A	A	A	A	R	D	D	D	D	D	D	D	D

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System I™ I/O and Sound Microprocessor Memory Map



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SP-276 Sheet 4A
1st printing

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**System I™ Main PCB
Schematic Diagram**

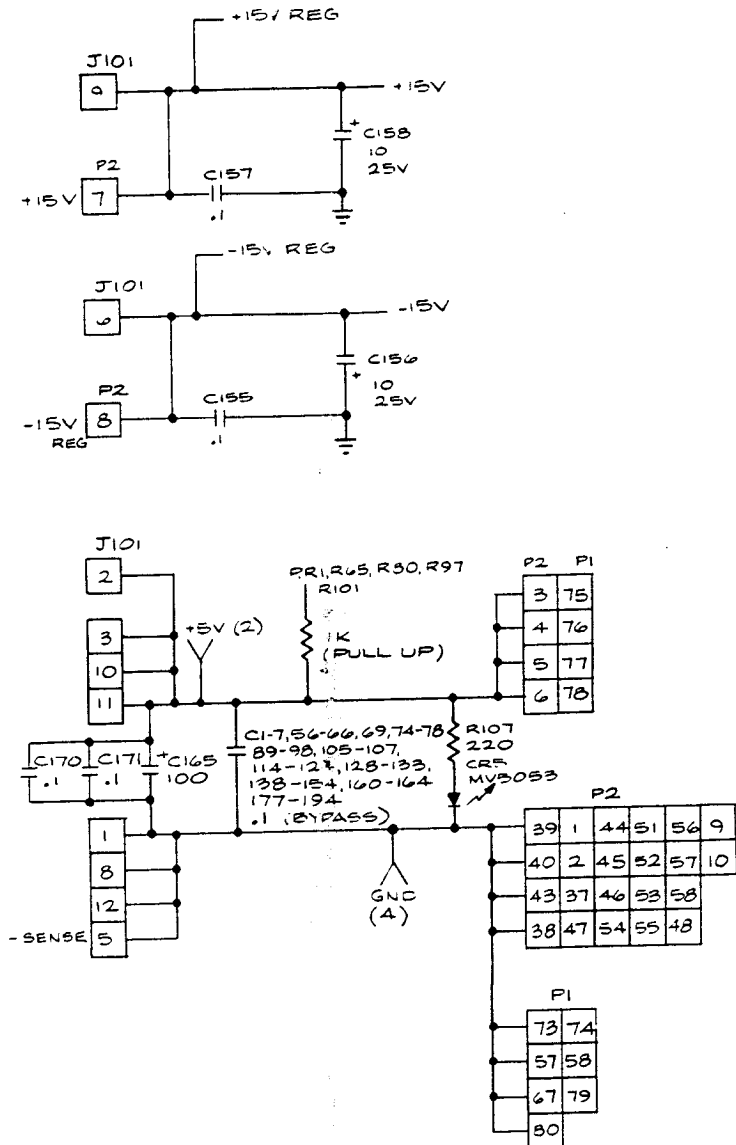


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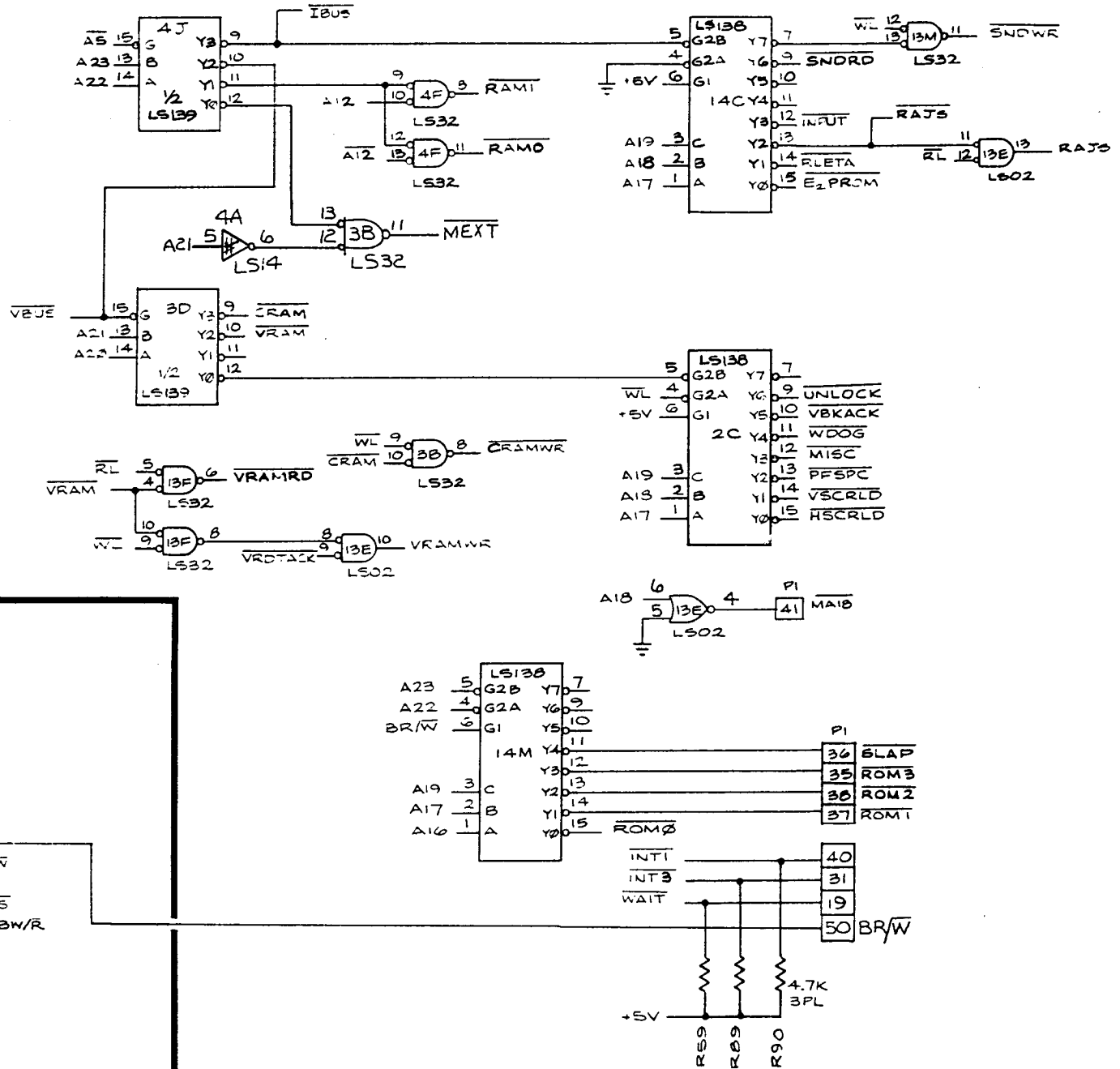
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**SP-277 Sheet 4B
1st printing**

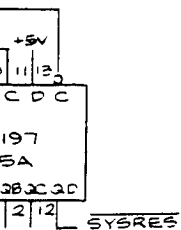
Power Input



Address Decoder



Watchdog and Reset

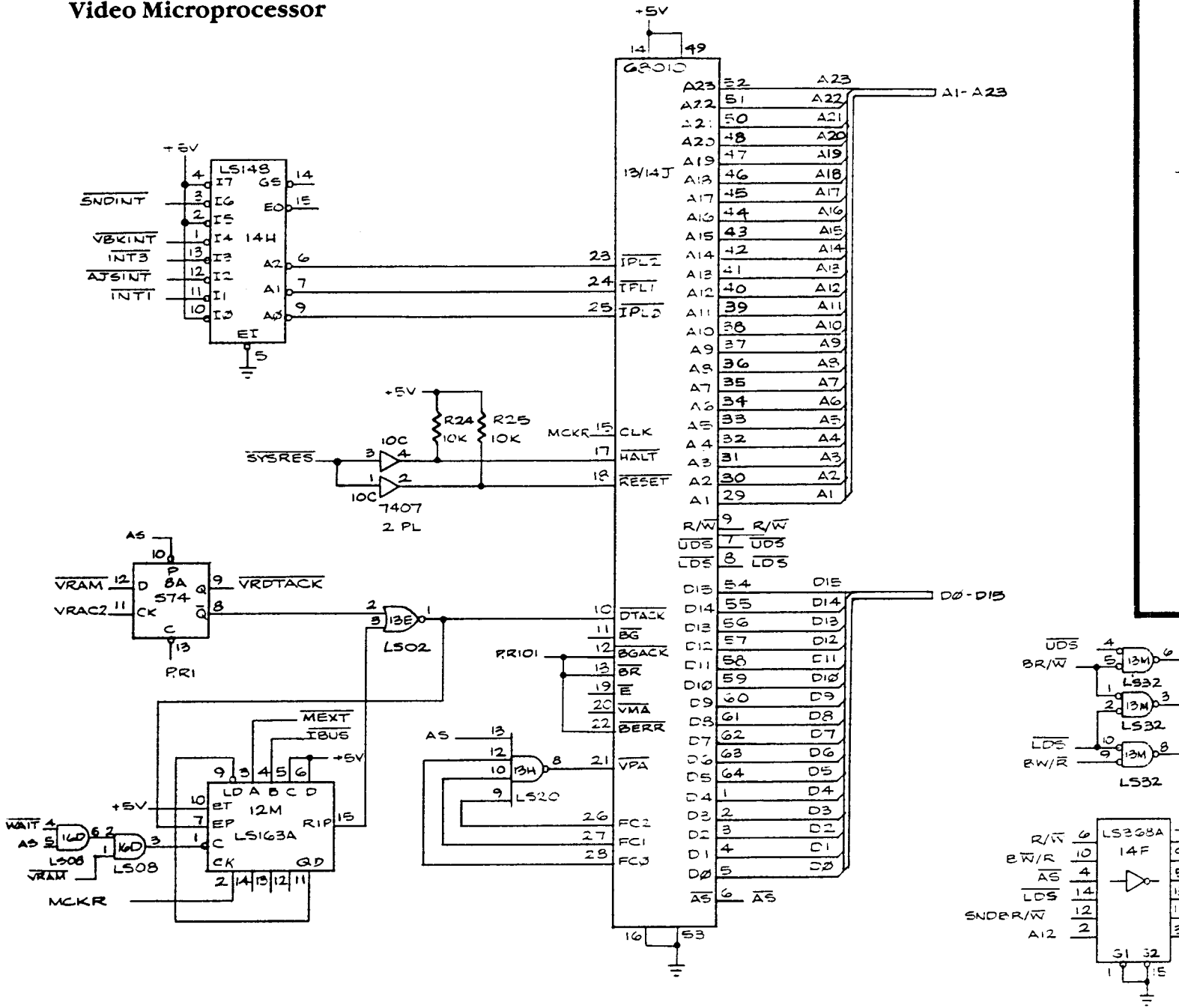


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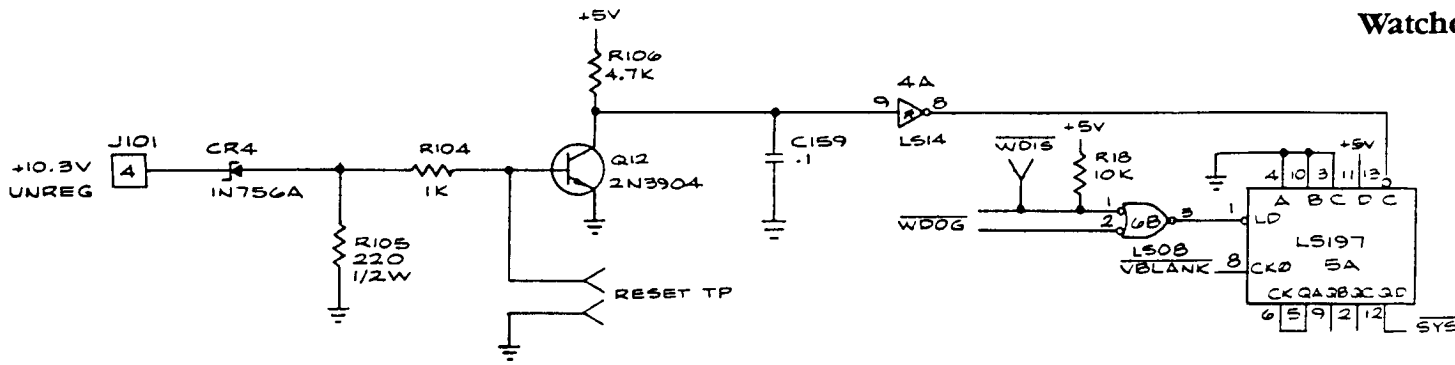
System I™ Main PCB Schematic Diagram



Video Microprocessor

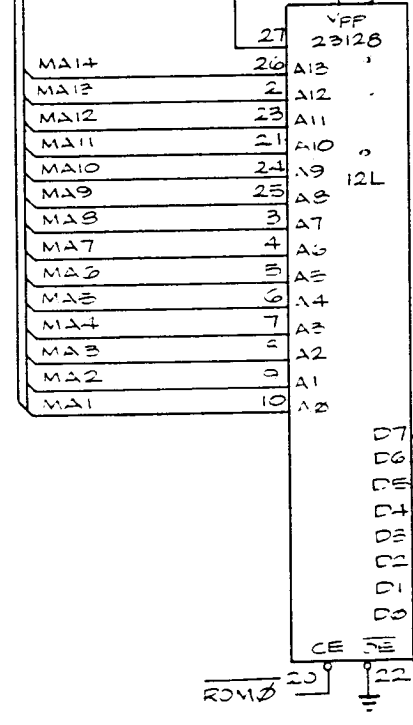
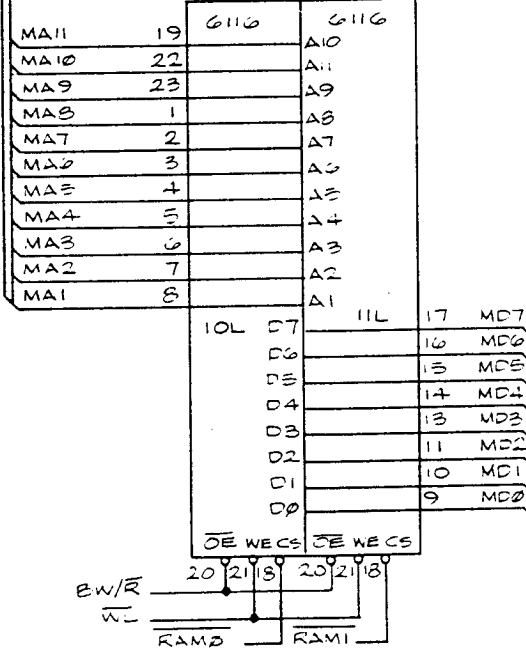
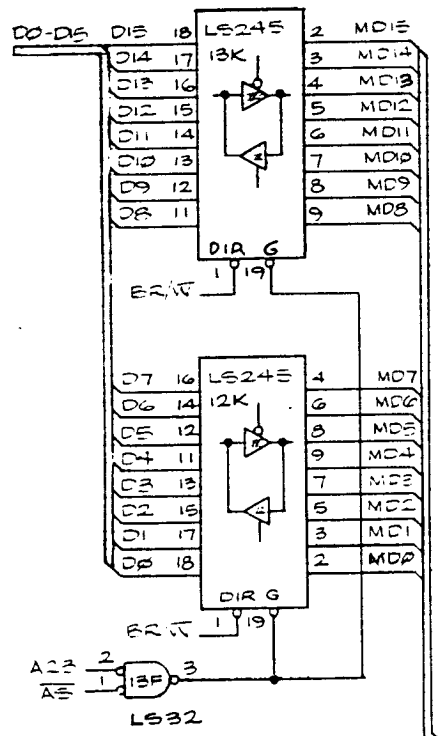
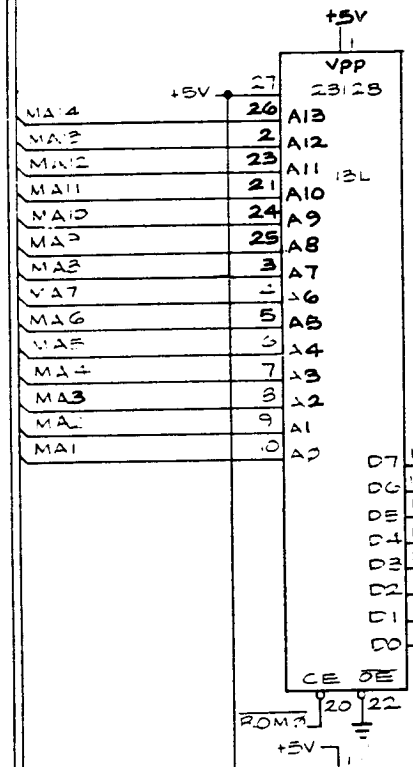
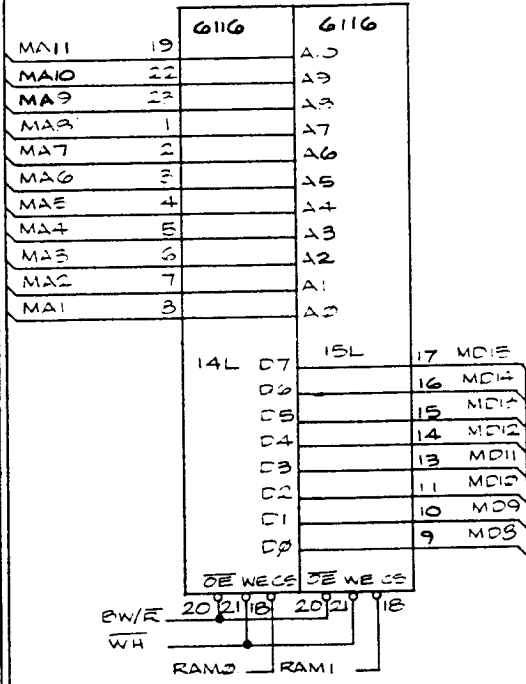
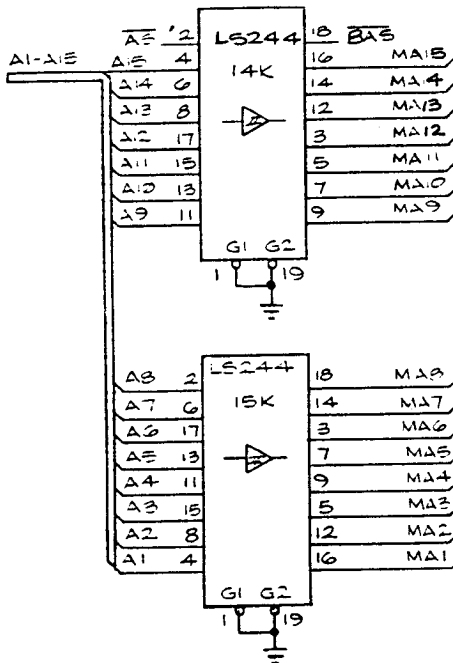


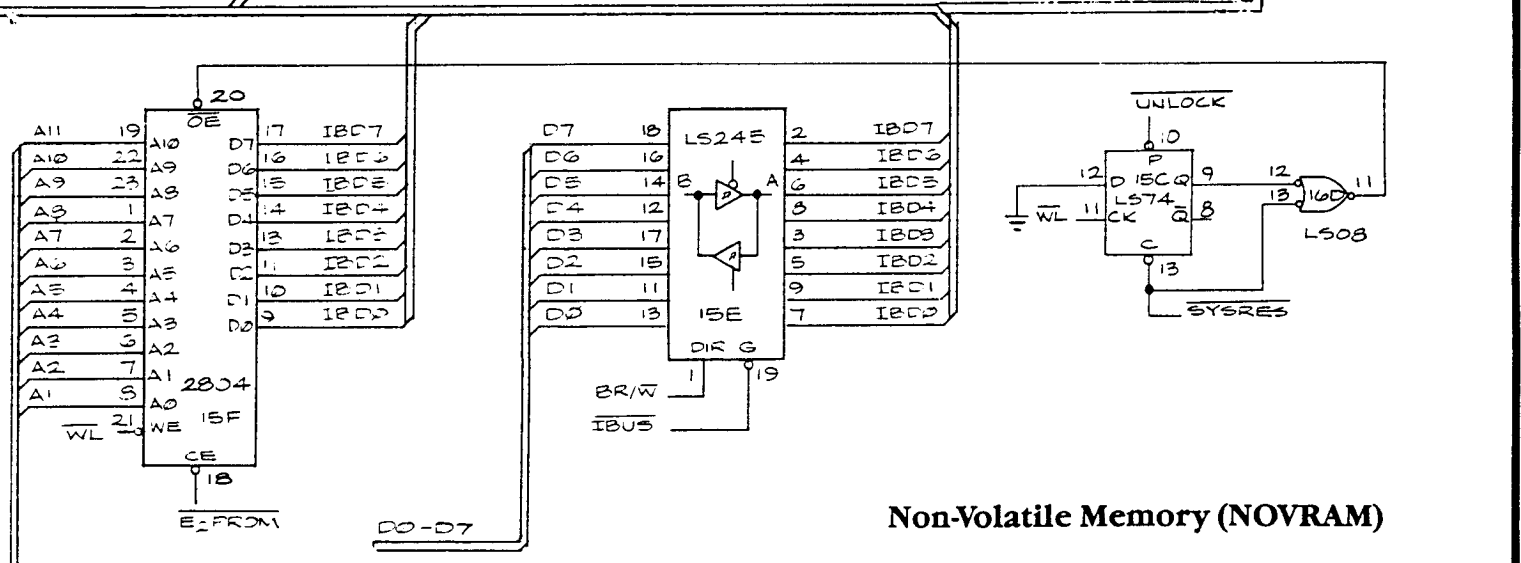
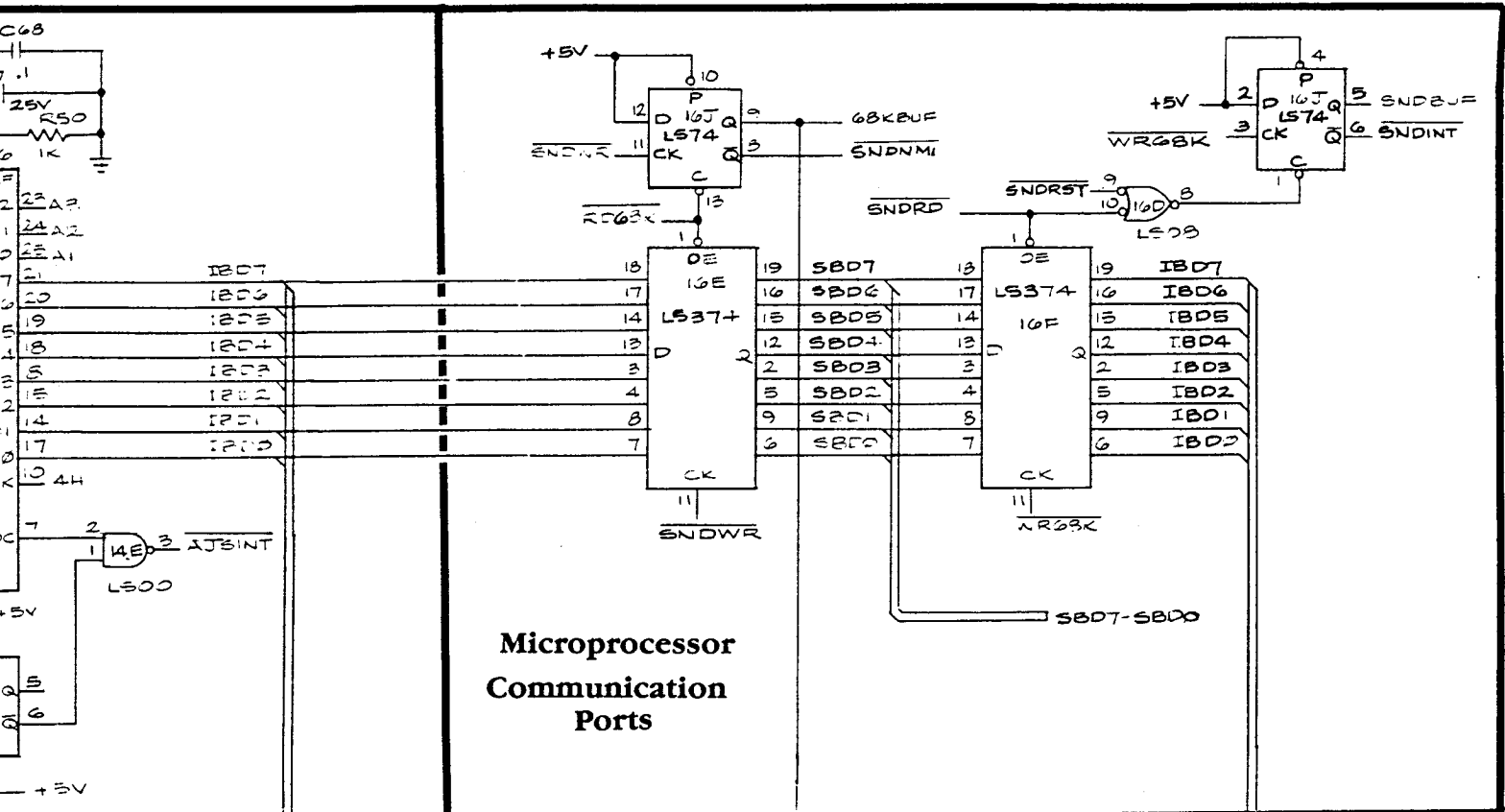
Watchdog



Video Microprocessor

Main Memory



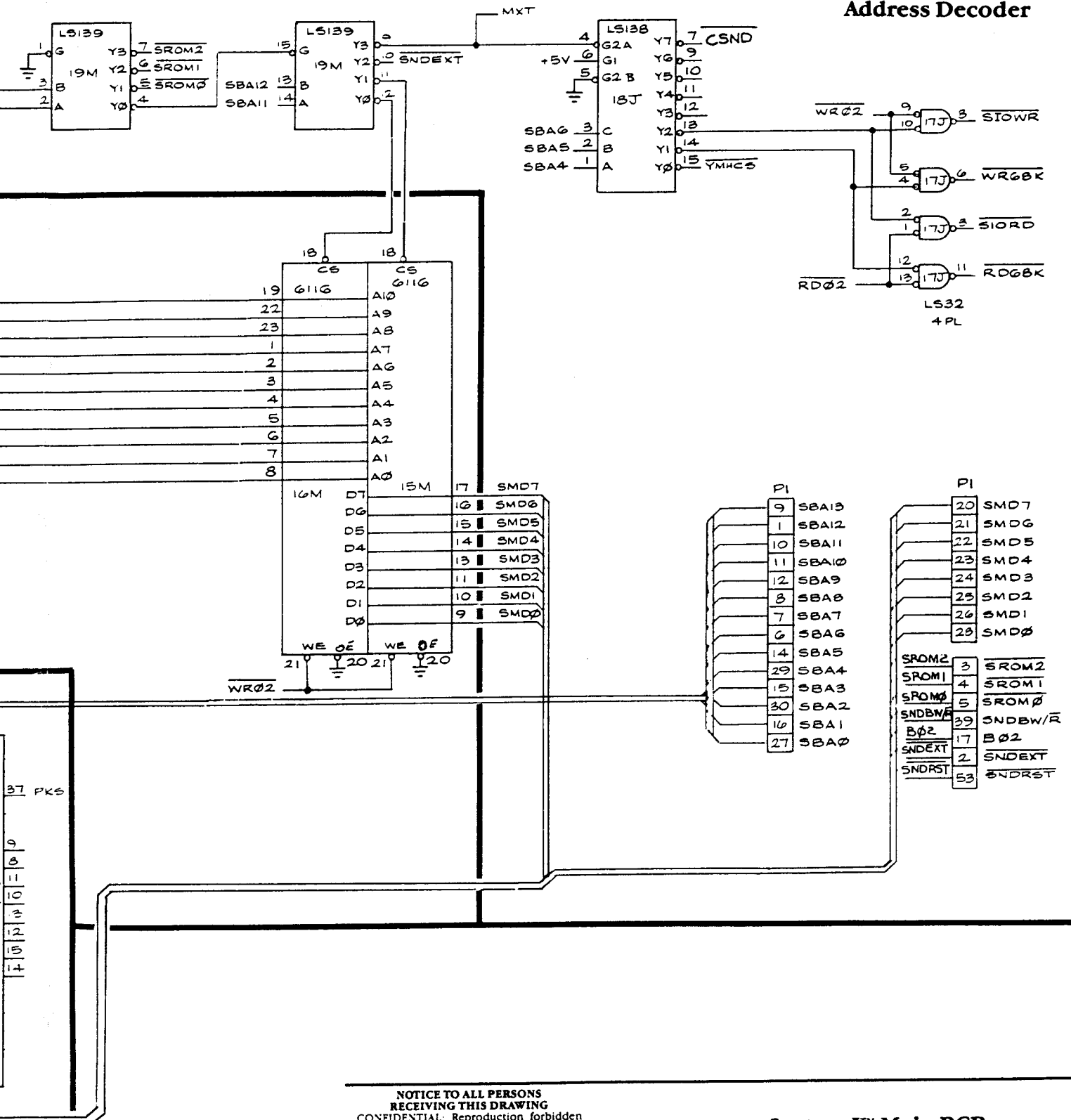


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System I™ Main PCB Schematic Diagram



Address Decoder



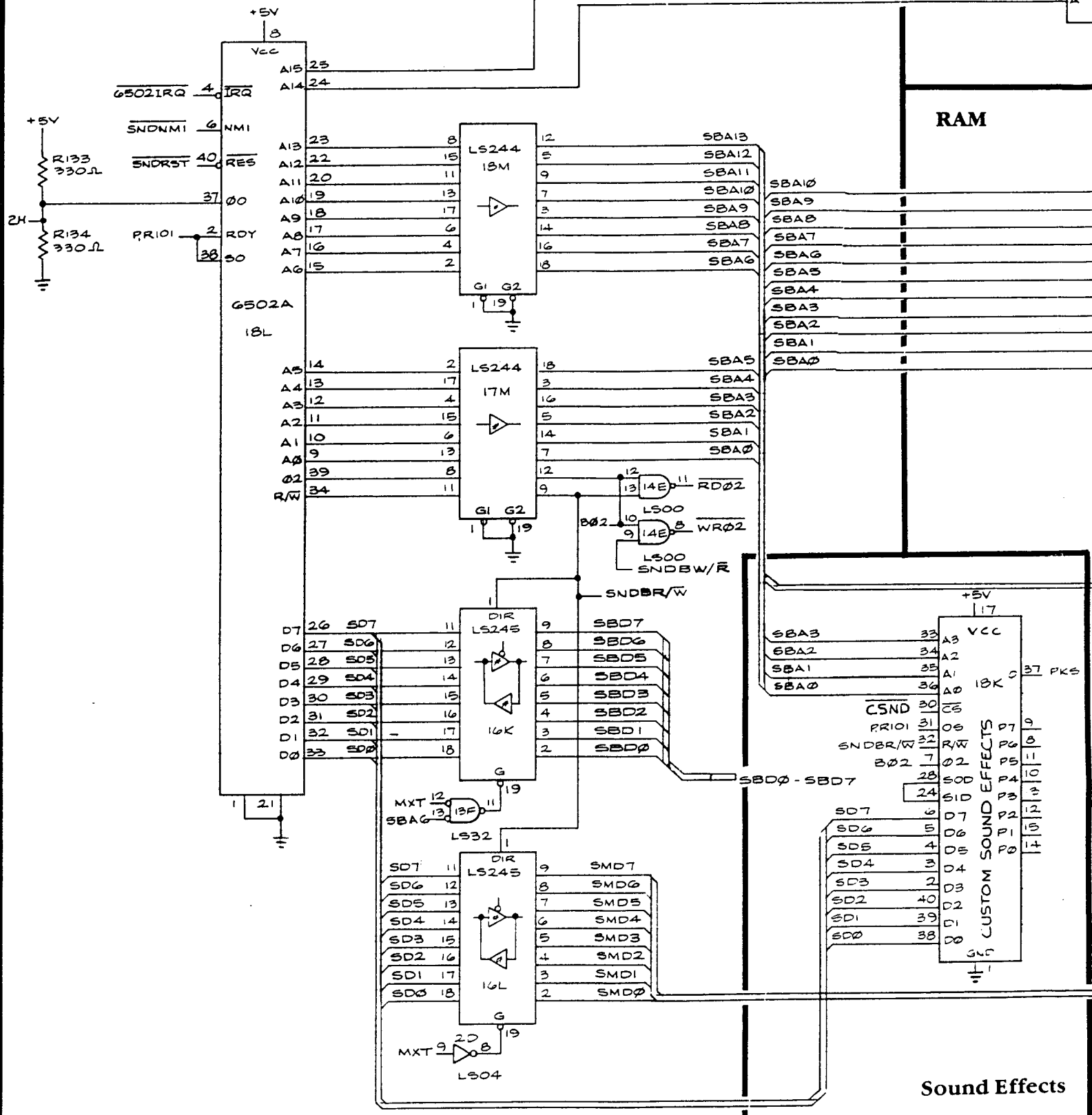
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System I™ Main PCB Schematic Diagram



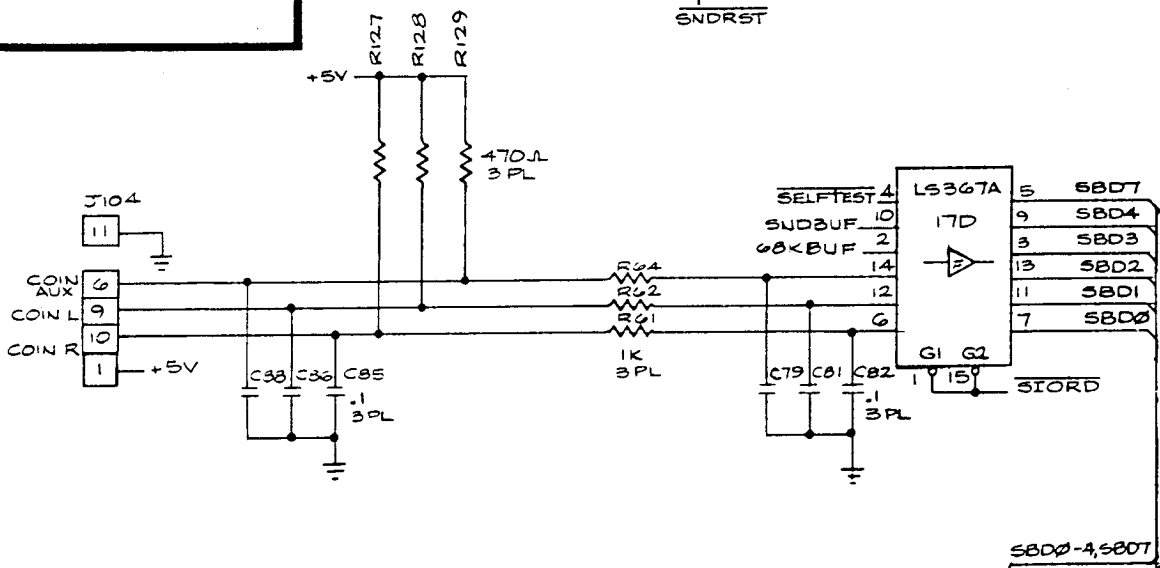
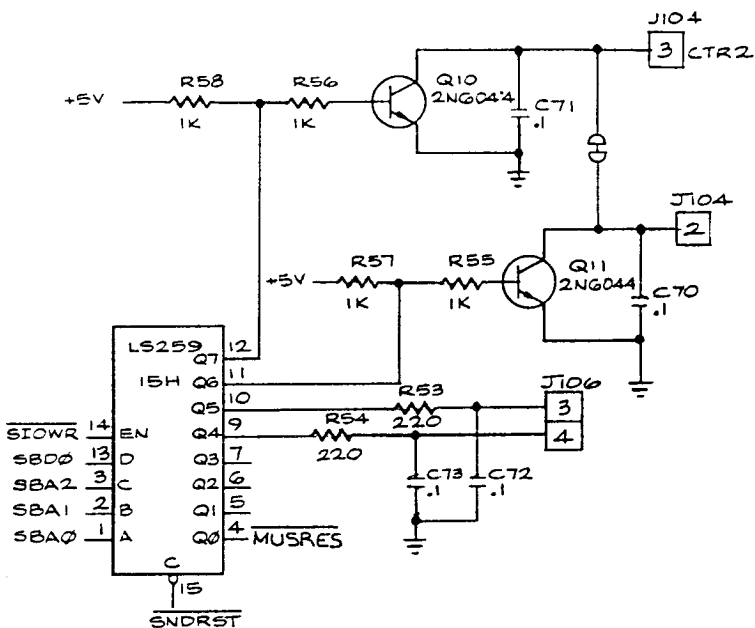
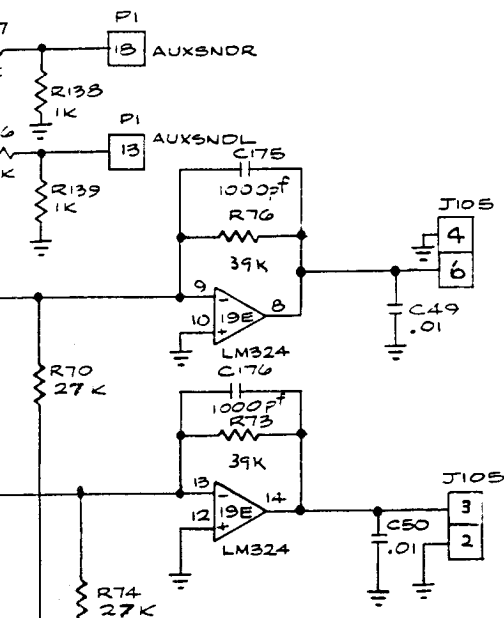
I/O and Sound Microprocessor



Sound Effects

sic

Coin I/O and LED



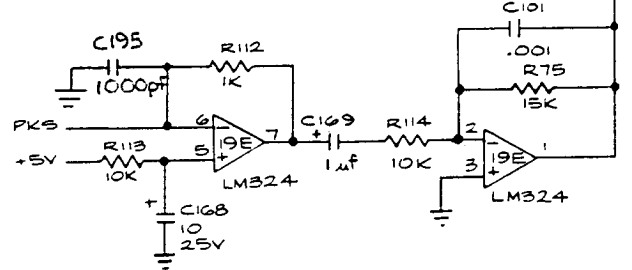
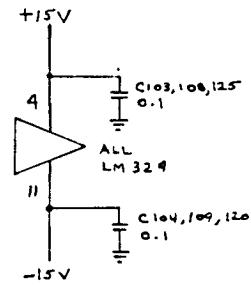
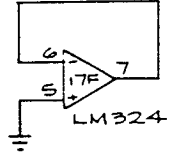
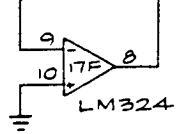
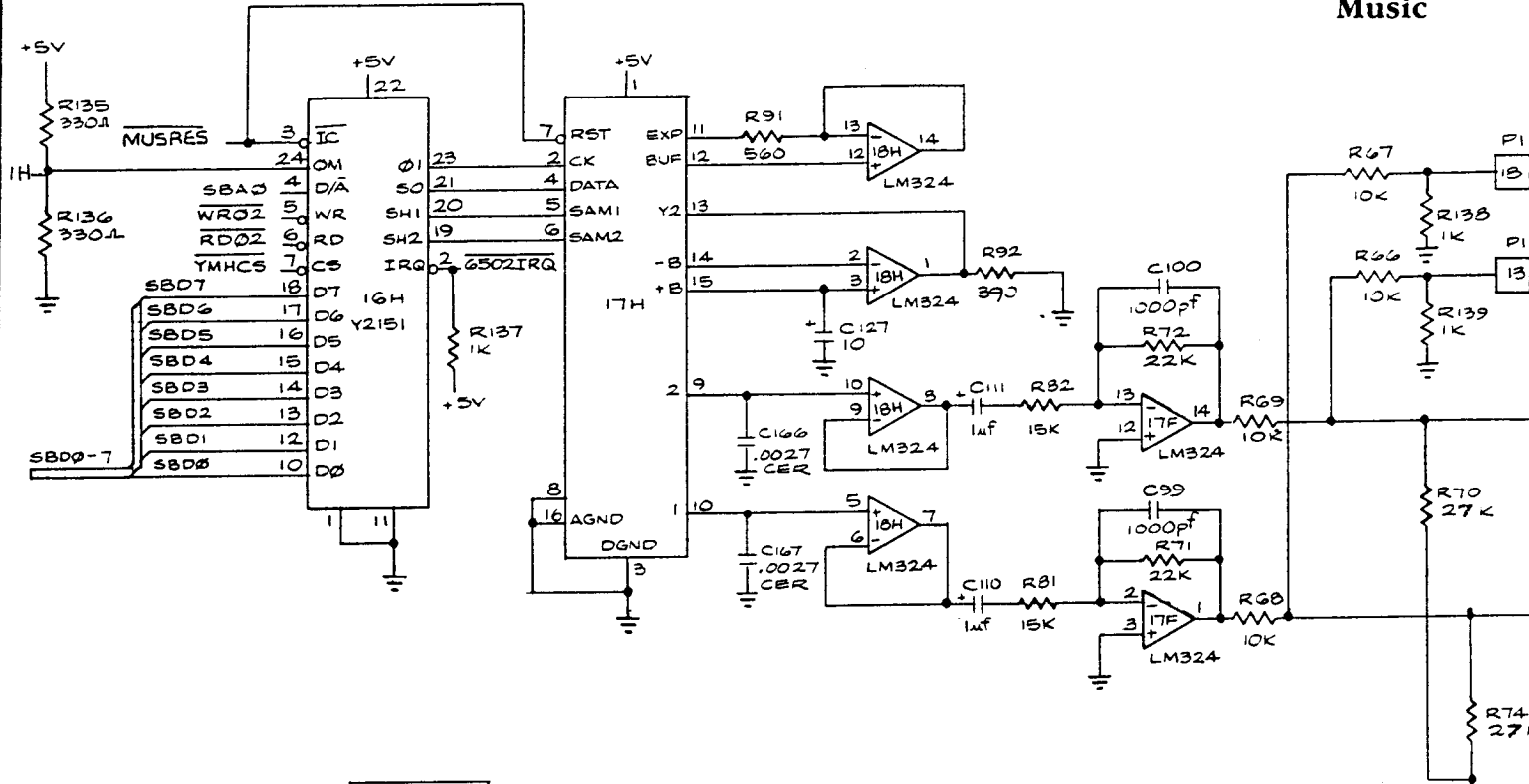
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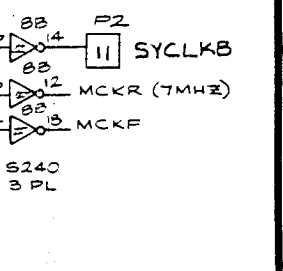
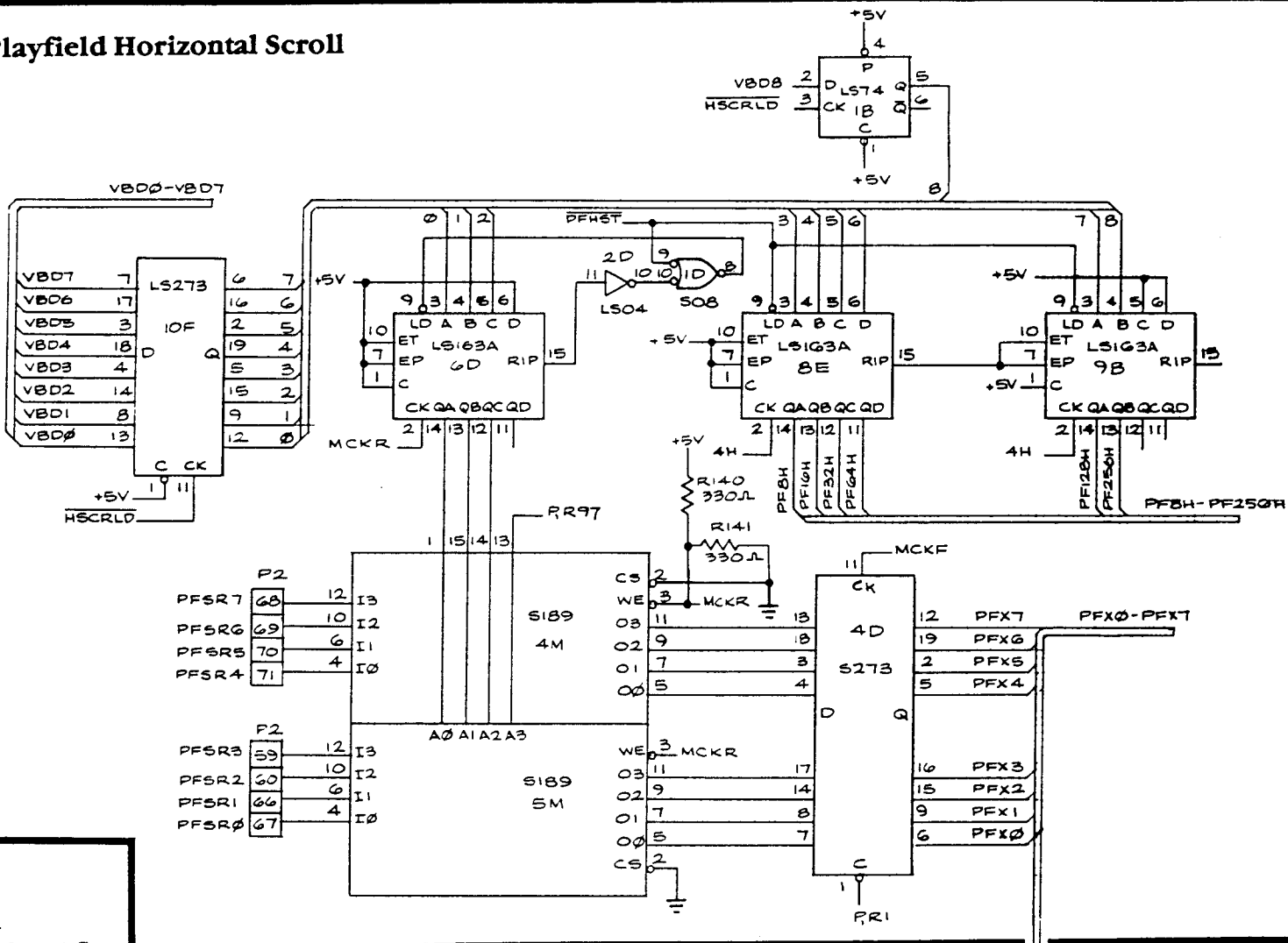
System I™ Main PCB Schematic Diagram



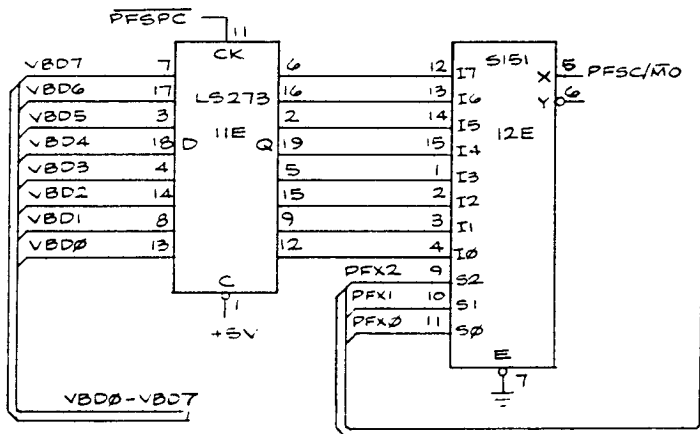
Music



Playfield Horizontal Scroll



Playfield Priority

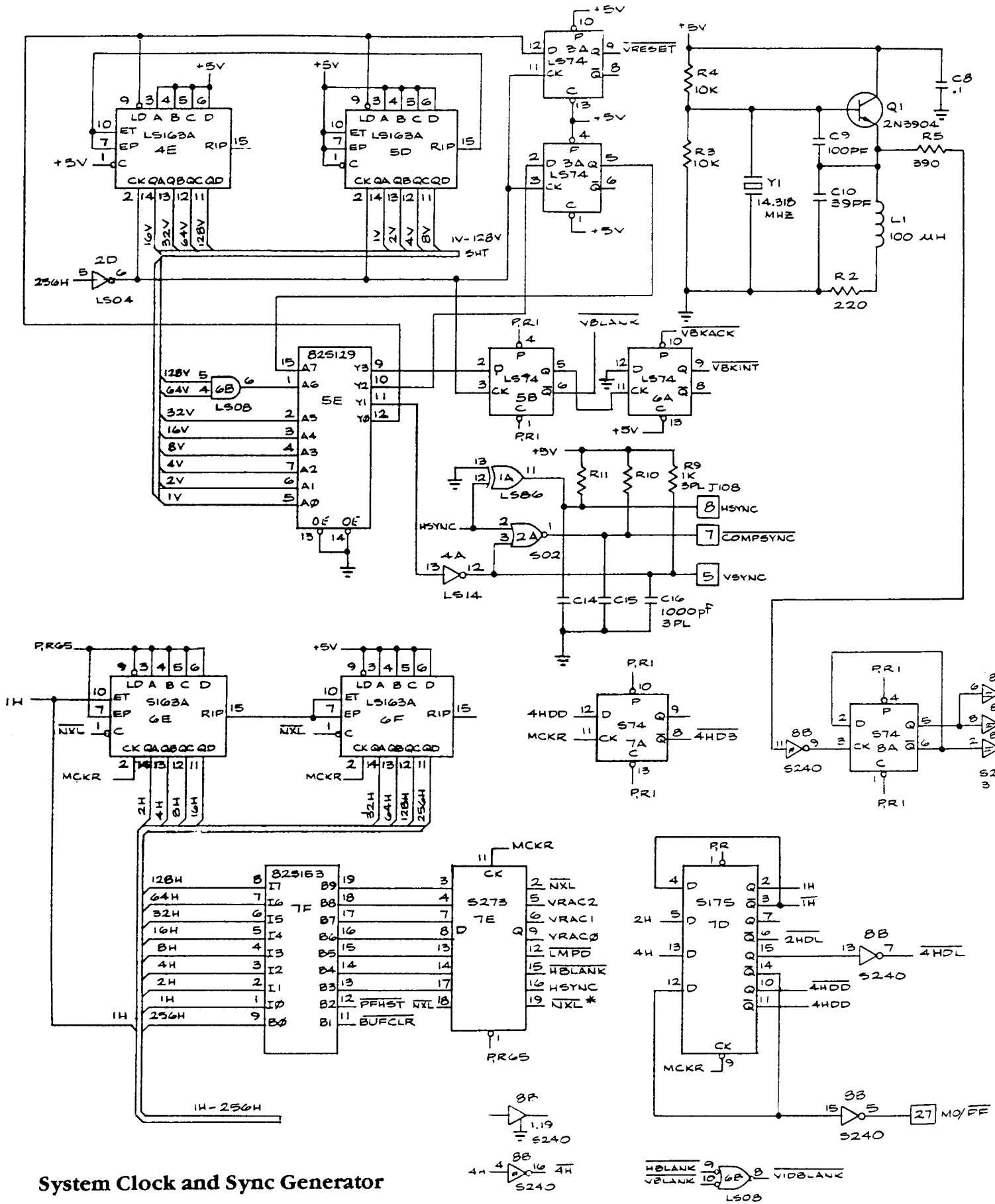


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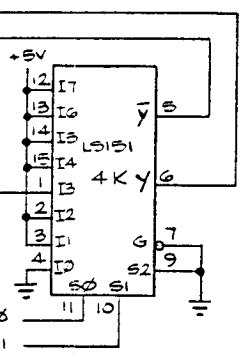
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System I™ Main PCB Schematic Diagram

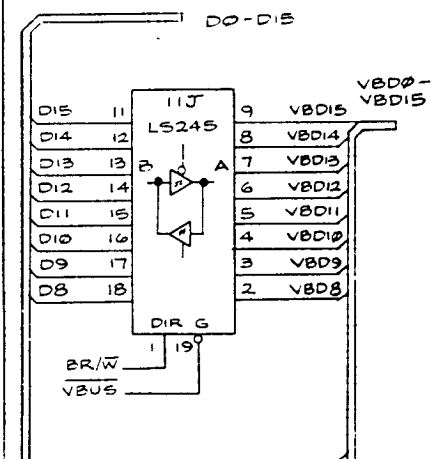
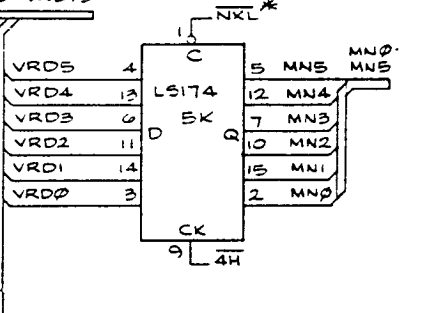
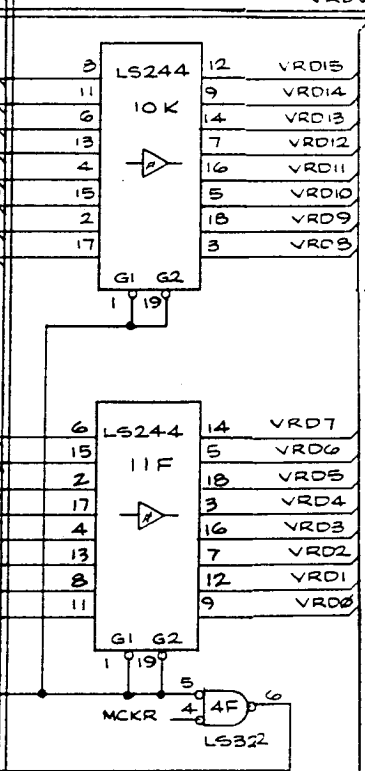
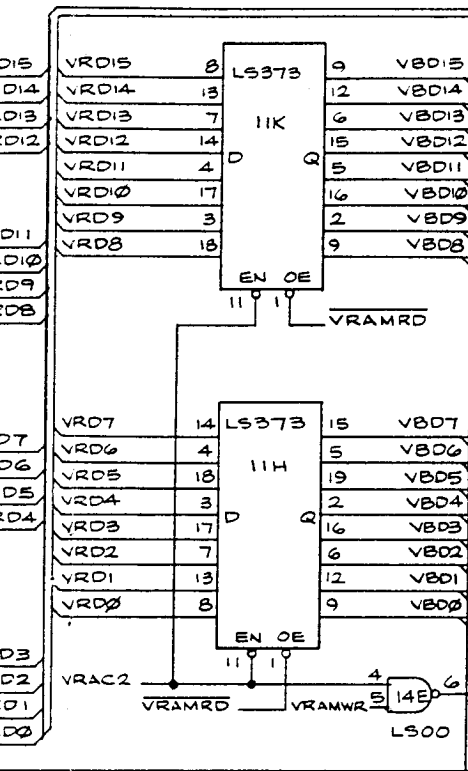
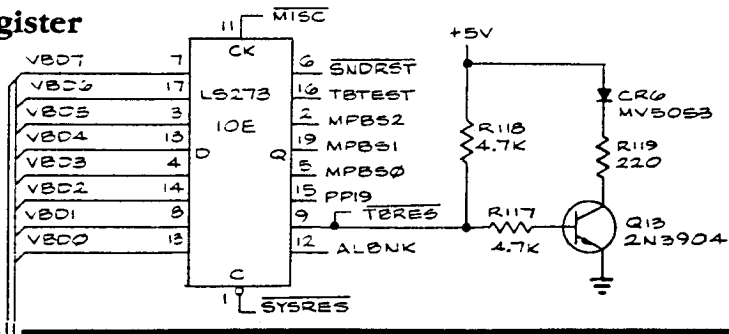




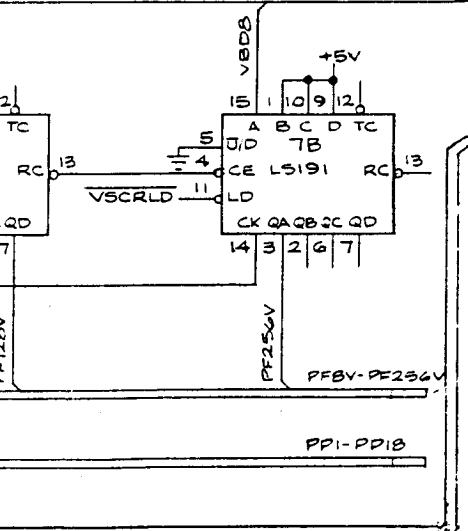
System Clock and Sync Generator



Control Register



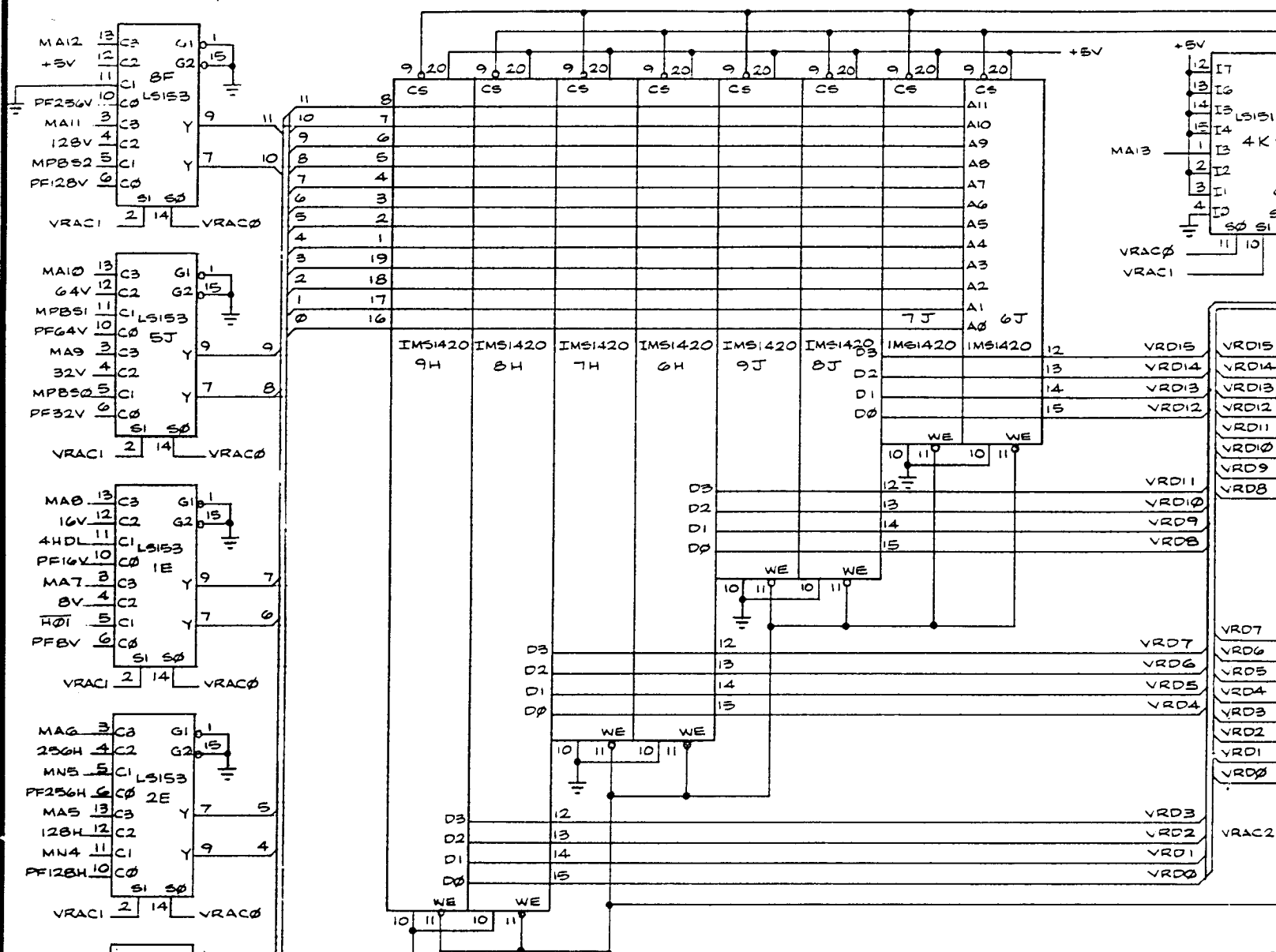
Data Buffer



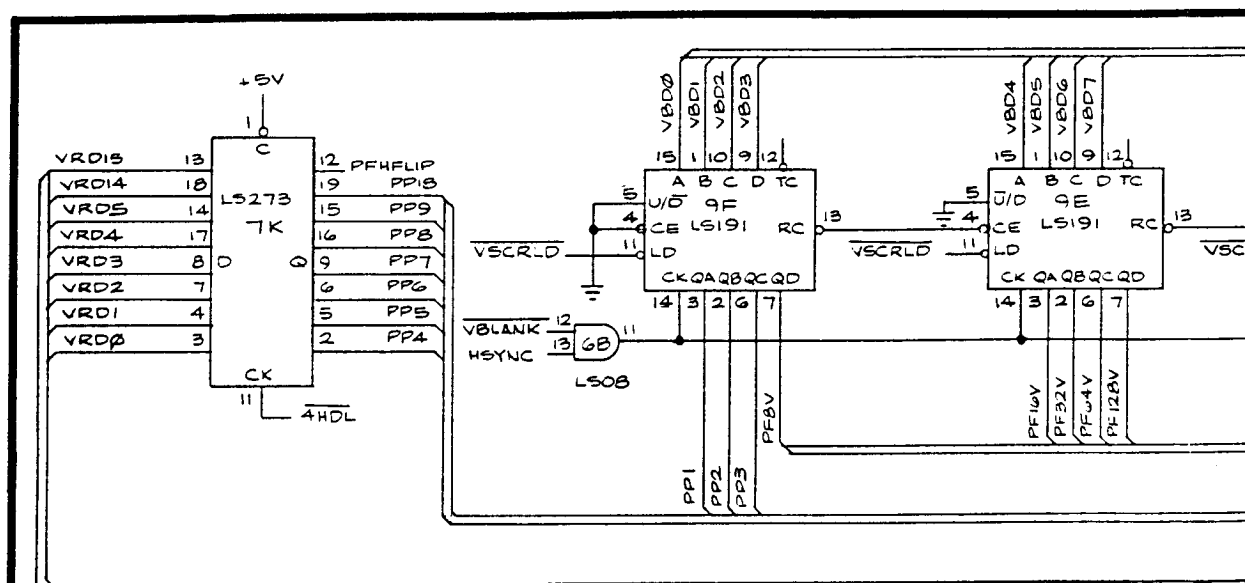
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System I™ Main PCB Schematic Diagram





Video RAM and Data Buf



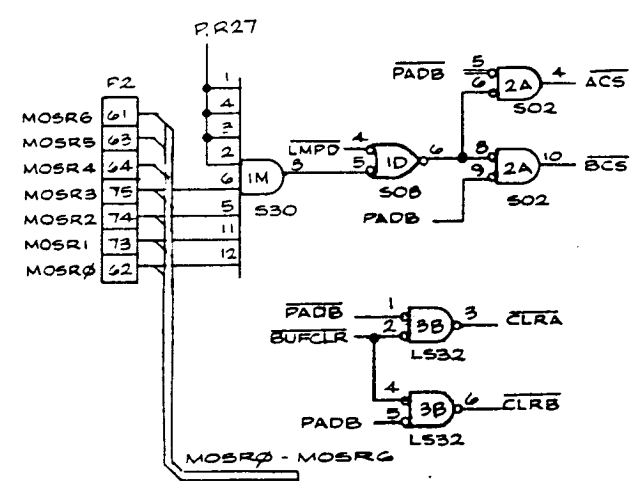
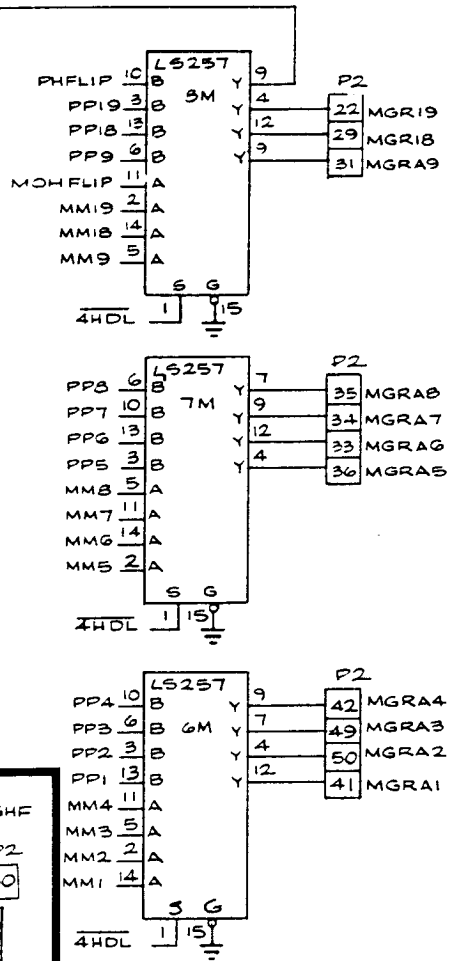
Playfield Vertical Scroll

Playfield

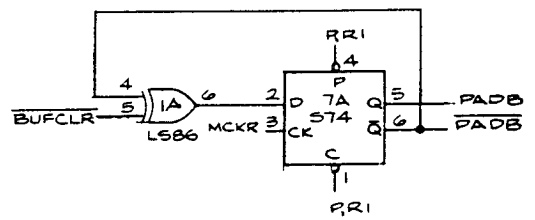
ress

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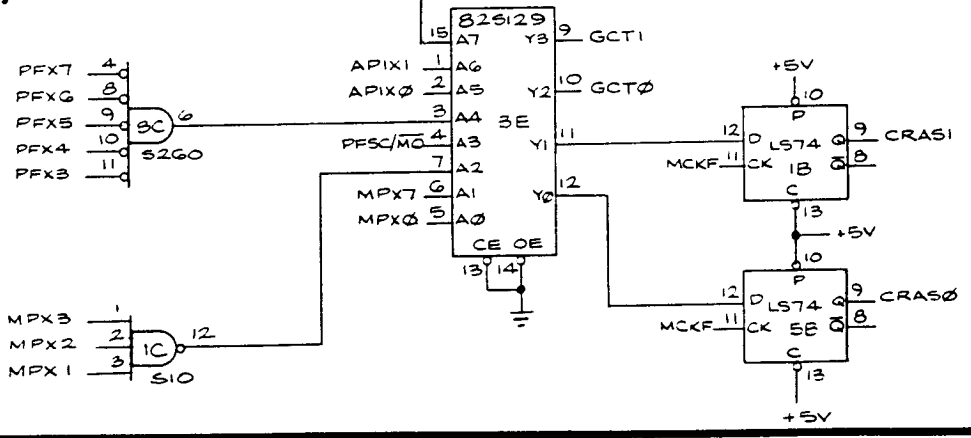
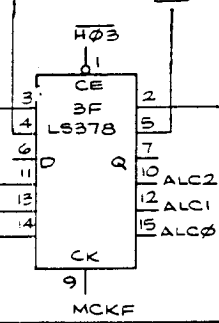
MM8



Motion Object Horizontal Line Buffer Control



Graphic Priority Control



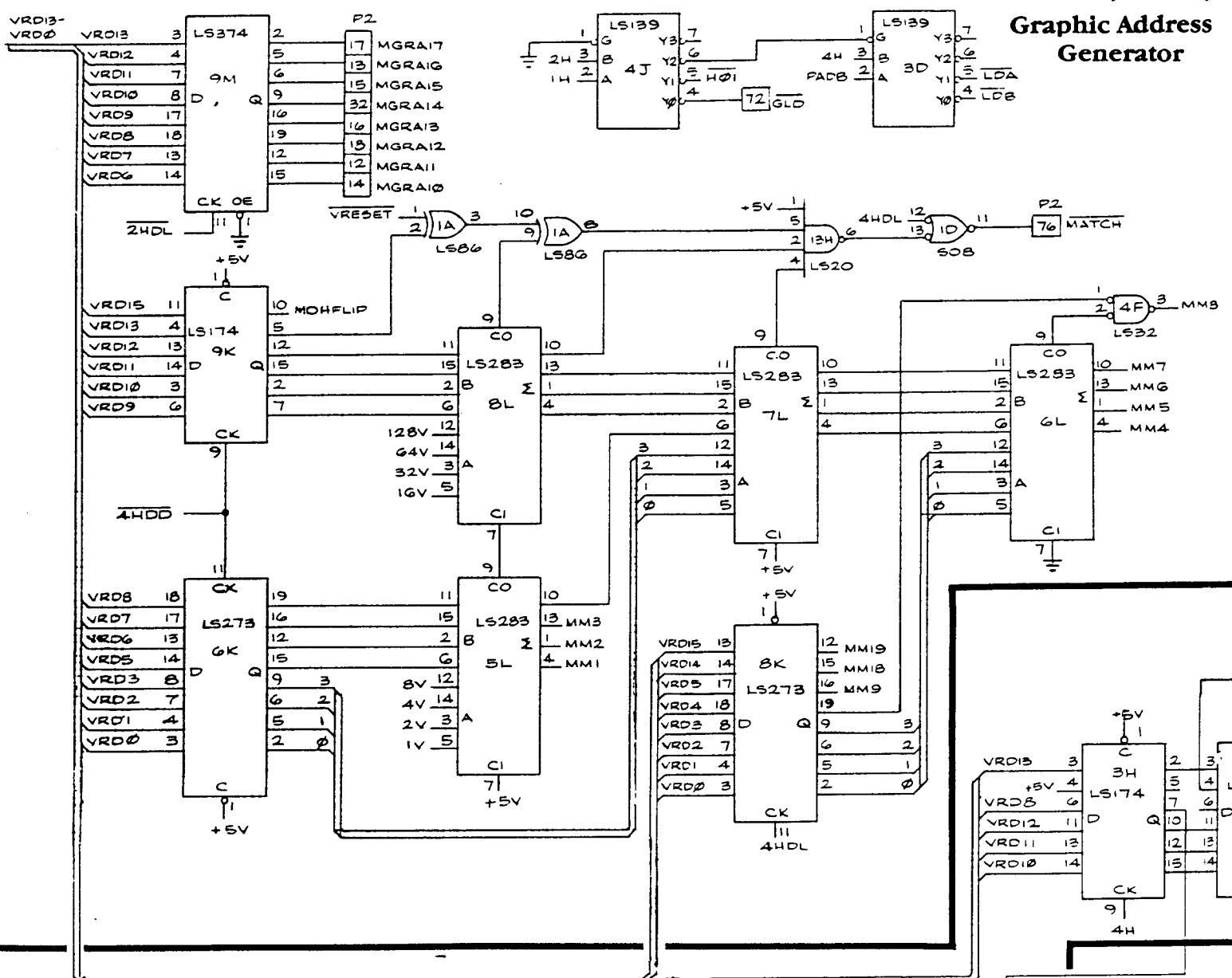
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System I™ Main PCB Schematic Diagram

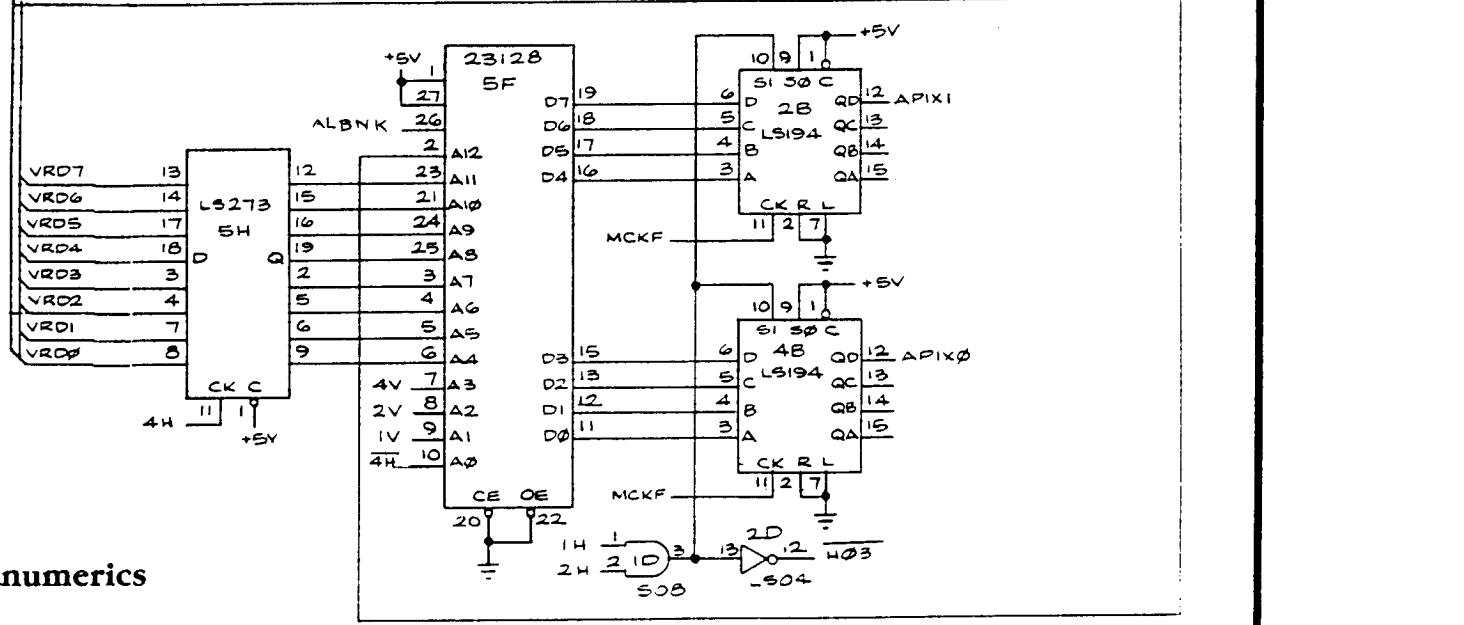


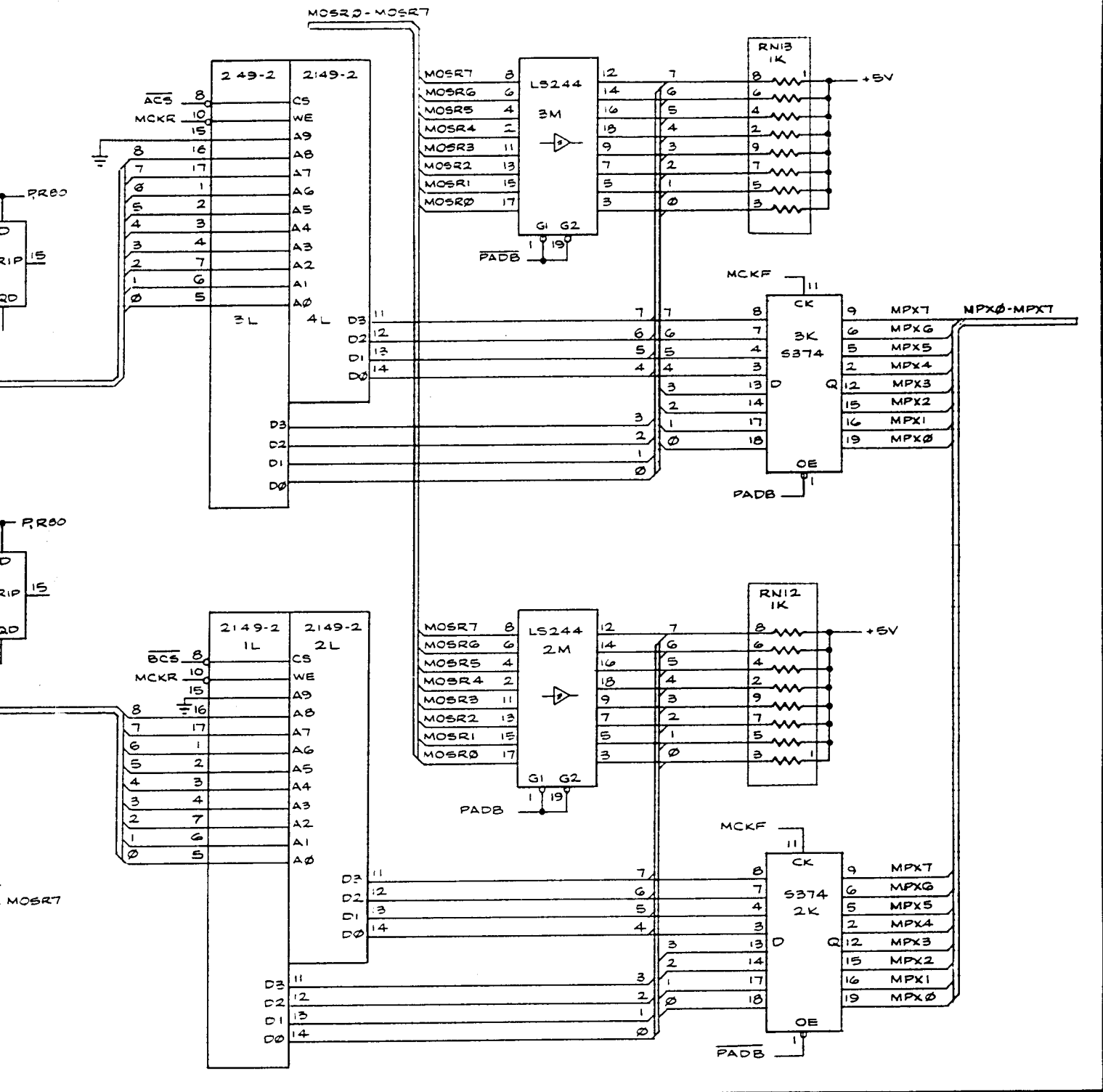
Motion Object/Playfield

Graphic Address Generator



Alphanumeric



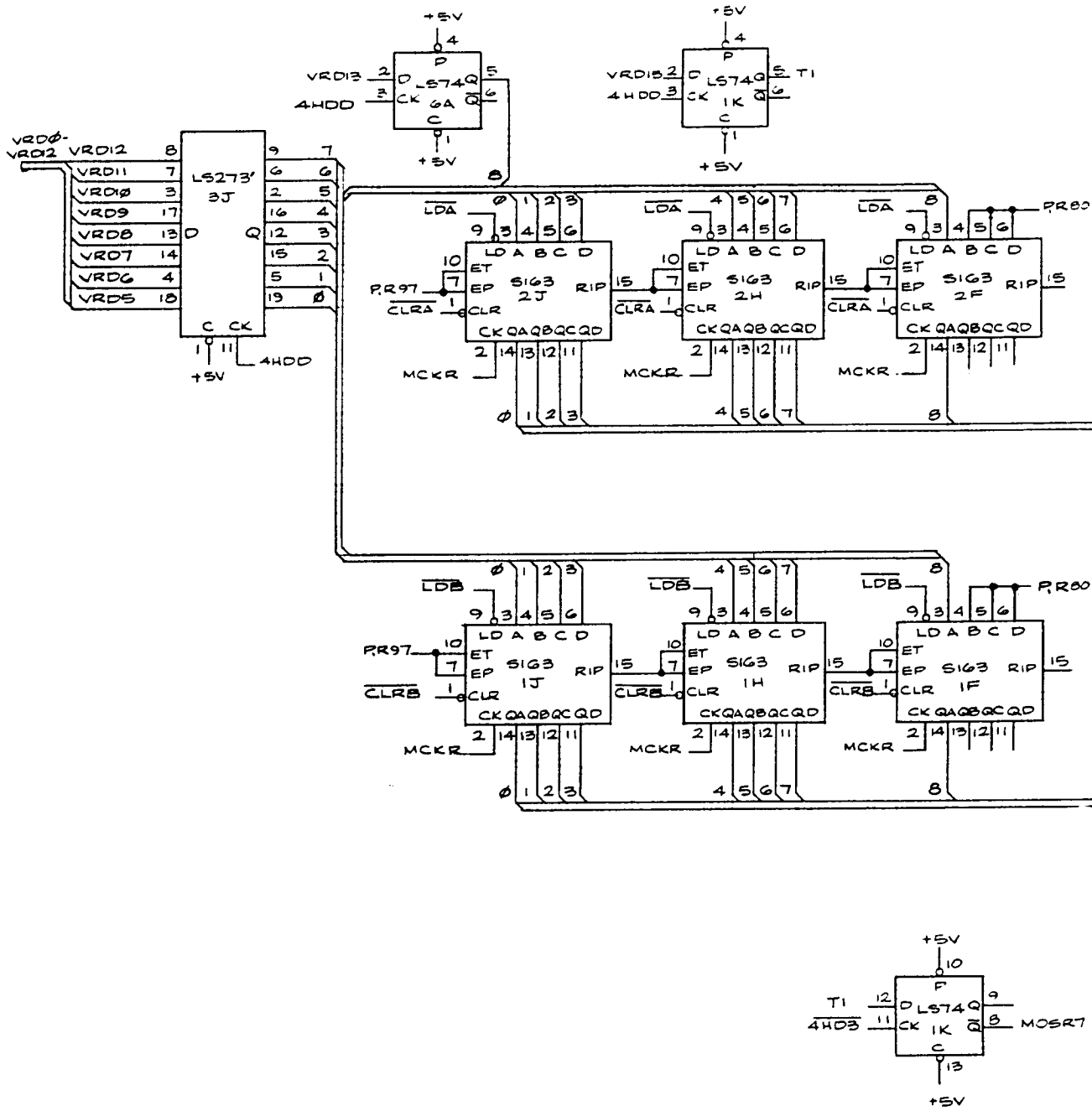


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System I™ Main PCB Schematic Diagram





Motion Object Horizontal Line Buffer

Color RAM

