

T-49-17-06

# UM6502E

PRELIMINARY

## 8-Bit Microprocessor

### Features

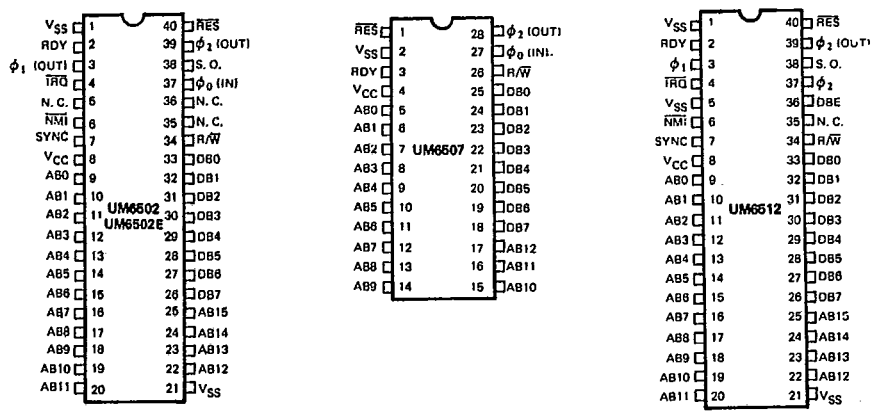
- UM6502E is the enhanced timing version of UM6502
- Single 5V ± 5% power supply
- N channel, silicon gate, depletion load technology
- 66 instructions
- Decimal and binary arithmetic
- Thirteen addressing modes
- True indexing capability
- Programmable stack pointer
- Variable length stack
- Interrupt capability
- Non-maskable Interrupt
- Bi-directional data bus
- Addressable memory range of up to 64K bytes
- "Ready" input
- Direct memory access capability
- Bus compatible with MC6800
- Choice of external or on-board clocks
- 1MHz, 2MHz, 3MHz and 4MHz versions
- On-chip clock options
  - External single clock input
  - Crystal time base input
- Pipeline architecture

### General Description

The UM6502/UM6502E/UM6507/UM6512 microprocessors are totally software compatible with one another. These products provide a selection of addressable memory range, interrupt input options and on-chip clock oscillators and drivers. The UM6502/UM6502E/UM6507 on-chip clock versions are aimed at high

performance, low cost applications where single phase inputs or crystals provide the time base. The UM6512 external clock version is geared for the multi-processor system applications where maximum timing control is mandatory. These products are bus compatible with the MC6800 product offering.

### Pin Configurations





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**Absolute Maximum Ratings\***

Supply Voltage  $V_{CC}$  ..... -0.3 to +7.0V  
 Input Voltage  $V_{in}$  ..... -0.3 to +7.0V  
 Operating Temperature  $T_A$  ..... 0 to 70°C  
 Storage Temperature  $T_{STG}$  ..... -55 to +150°C

**\*Comments**

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Microprocessor

**D.C. Electrical Characteristics** ( $V_{CC} = 5.0V \pm 5\%$ ,  $T_A = 0 - 70^\circ C$ )  
 ( $\phi_1, \phi_2$  applies to UM6512,  $\phi_0(in)$  applies to UM6502/UM6502E/UM6507)

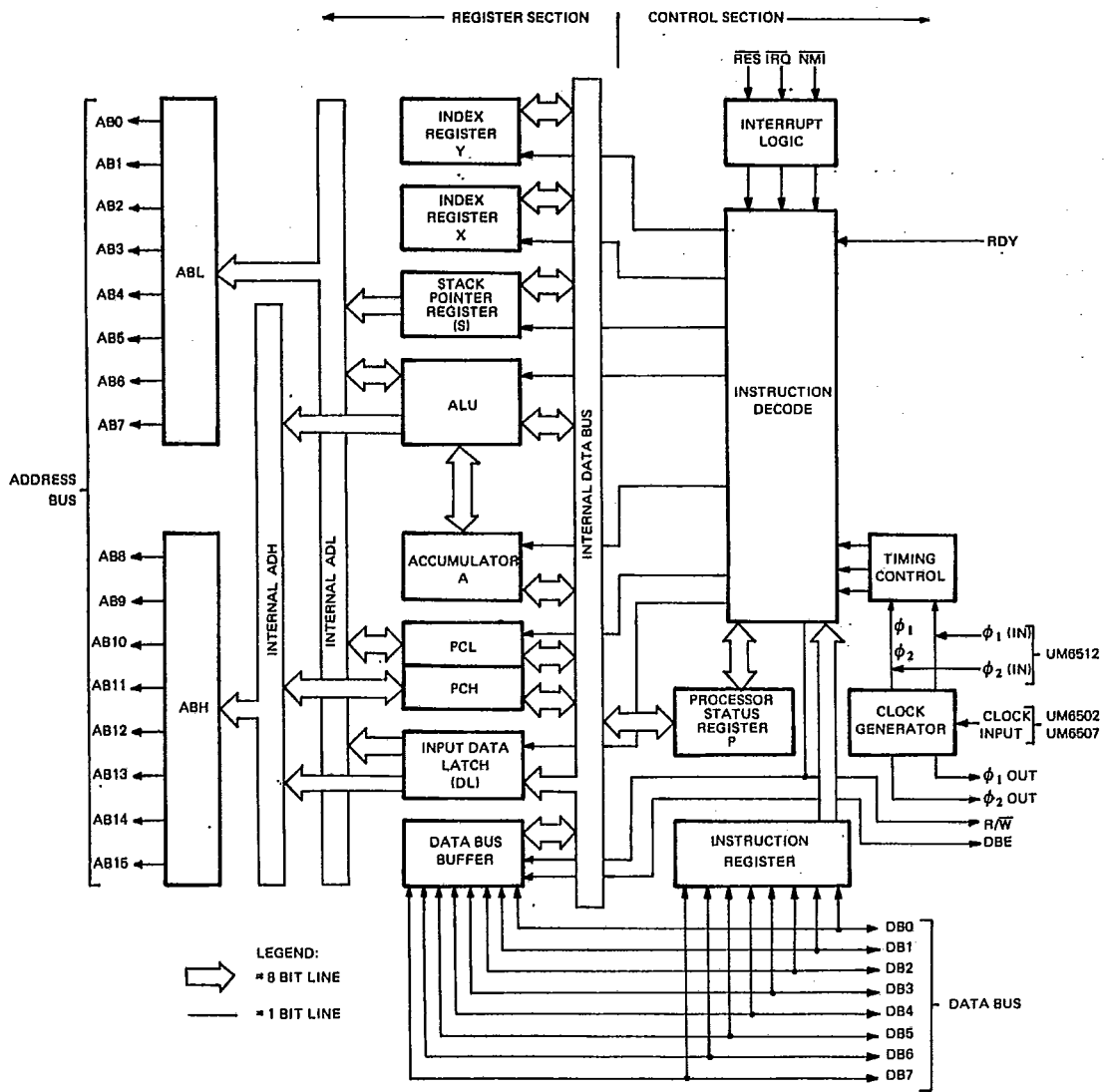
Symbol	Characteristics	Min.	Max.	Unit	
$V_{IH}$	Input High Voltage				
	Logic and $\phi_0$ (in) for UM6502/UM6502E/UM6507 } { 1, 2, 3 MHz	+ 2.0	$V_{CC}$	V	
	$\phi_1$ and $\phi_2$ only for UM6512 } { 4 MHz	+ 3.3	$V_{CC}$	V	
	All Speeds	$V_{CC} - 0.5$	$V_{CC} + 0.25$	V	
$V_{IL}$	Input Low Voltage				
	Logic, $\phi_0$ (in) (UM6502/UM6502E/UM6507) $\phi_1, \phi_2$ (UM6512)	-0.3 -0.3	+0.8 +0.2	V	
$I_{IL}$	Input Loading ( $V_{in} = 0V, V_{CC} = 5.25V$ ) RDY, S.O.	-10	-300	$\mu A$	
$I_{in}$	Input Leakage Current ( $V_{in} = 0$ to 5.25 V, $V_{CC} = 0$ )	-	2.5	$\mu A$	
	Logic (Excl. RDY, S.O.)	-	100	$\mu A$	
	$\phi_1, \phi_2$ (UM6512)	-	10.0	$\mu A$	
	$\phi_0$ (in) (UM6502/UM6502E/UM6507)	-			
$I_{TSI}$	Three-State (Off State) Input Current ( $V_{in} = 0.4$ to 2.4 V, $V_{CC} = 5.25V$ ) DB0-DB7	-	$\pm 10$	$\mu A$	
$V_{OH}$	Output High Voltage ( $I_{LOAD} = -100 \mu A_{dc}, V_{CC} = 4.75V$ ) 1, 2 MHz SYNC, DB0-DB7, AB0-AB15, $R/\bar{W}$	2.4	-	V	
$V_{OL}$	Output Low Voltage ( $I_{LOAD} = 1.6mA_{dc}, V_{CC} = 4.75V$ ) 1, 2 MHz SYNC, DB0-DB7, AB0-AB15, $R/\bar{W}$	-	0.4	V	
$P_D$	Power Dissipation 1MHz and 2 MHz ( $V_{CC} = 5.25V$ )	-	700	mW	
C	Capacitance ( $V_{in} = 0, T_A = 25^\circ C, f = 1 MHz$ )				
	$C_{in}$	RES, NMI, RDY, $\bar{TRQ}$ , S.O., DBE DB0-DB7	-	10 15	pF
	$C_{out}$	AB0-AB15, $R/\bar{W}$ , SYNC	-	12	
	$C_{\phi_0}(in)$	$\phi_0$ (in) (UM6502/UM6502E/UM6507)	-	15	
	$C_{\phi_1}$	$\phi_1$ (UM6512)	-	50	
	$C_{\phi_2}$	$\phi_2$ (UM6512)	-	80	



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Block Diagram



Notes: 1. Clock generator is not included on UM6512.  
 2. Addressing capability and control options vary with each product.

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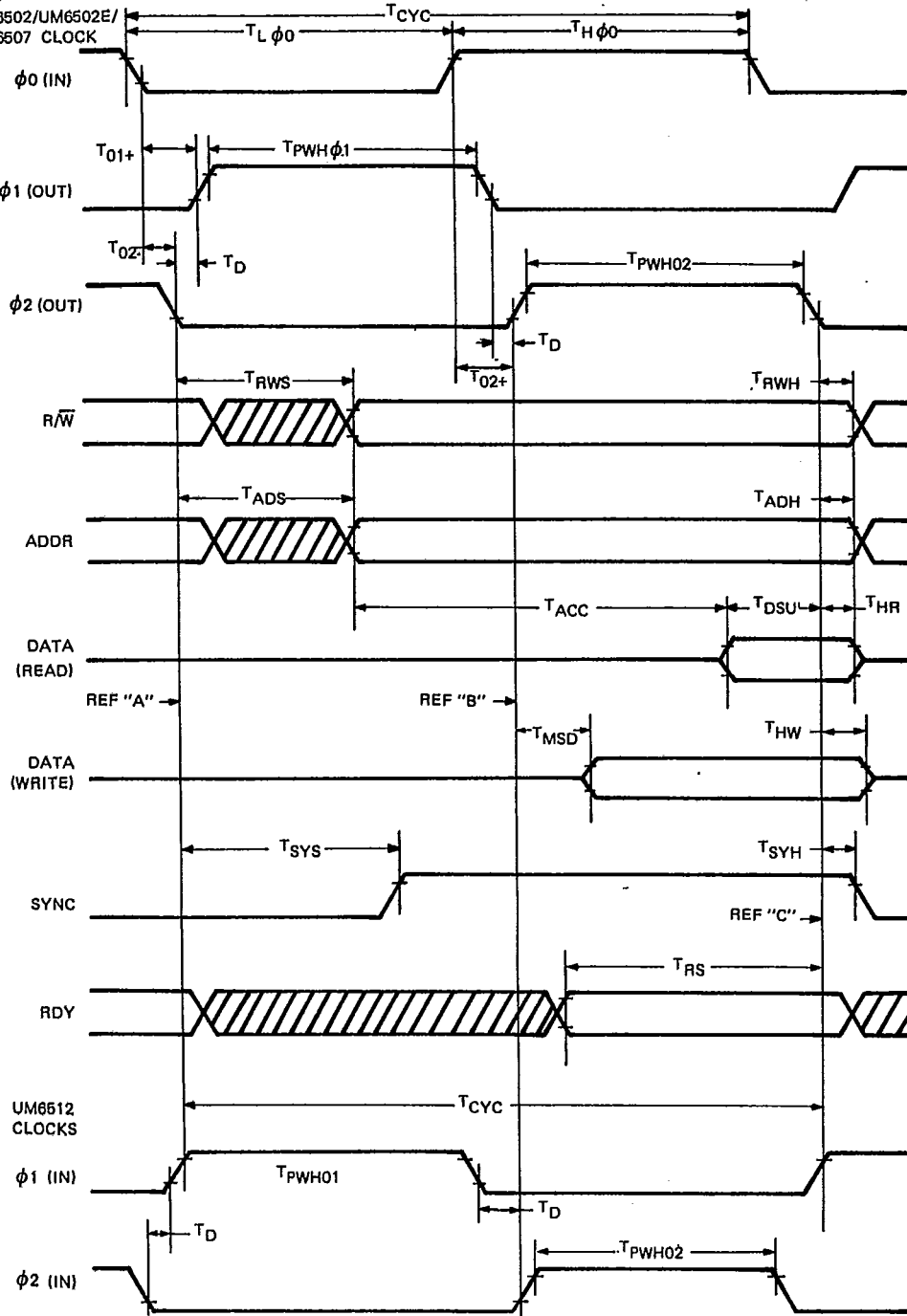


UM6502E

Microprocessor

**Timing Waveforms**

UM6502/UM6502E/  
UM6507 CLOCK





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Dynamic Operating Characteristics ( $V_{CC} = 5.0 \pm 5\%$ ,  $T_A = 0^\circ$  to  $70^\circ\text{C}$ )

Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>UM6502E</b>										
Cycle Time	$T_{CYC}$	1.00	40	0.50	40	0.33	40	0.25	40	$\mu\text{s}$
$\phi_0$ (IN) Low Time <sup>(2)</sup>	$T_{L\phi_0}$	480	—	240	—	160	—	110	—	ns
$\phi_0$ (IN) High Time <sup>(2)</sup>	$T_{H\phi_0}$	460	—	240	—	160	—	115	—	ns
$\phi_0$ Neg to $\phi_1$ Pos Delay <sup>(5)</sup>	$T_{01+}$	10	70	—	50	—	45	—	35	ns
$\phi_0$ Neg to $\phi_2$ Neg Delay <sup>(5)</sup>	$T_{02-}$	5	65	—	45	—	40	—	35	ns
$\phi_0$ Pos to $\phi_1$ Neg Delay <sup>(5)</sup>	$T_{01-}$	5	65	—	45	—	40	—	30	ns
$\phi_0$ Pos to $\phi_2$ Pos Delay <sup>(5)</sup>	$T_{02+}$	15	75	—	45	—	45	—	35	ns
$\phi_0$ (IN) Rise and Fall Time <sup>(1)</sup>	$T_{RO}, T_{FO}$	0	30	—	20	—	15	—	10	ns
$\phi_1$ (OUT), Pulse Width	$T_{PWH\phi_1}$	$T_{L\phi_0} - 20$	$T_{L\phi_0}$	$T_{L\phi_0} - 20$	$T_{L\phi_0}$	$T_{L\phi_0} - 20$	$T_{L\phi_0}$	$T_{L\phi_0} - 20$	$T_{L\phi_0}$	ns
$\phi_2$ (OUT), Pulse Width	$T_{PWH\phi_2}$	$T_{L\phi_0} - 40$	$T_{L\phi_0} - 10$	$T_{L\phi_0} - 40$	$T_{L\phi_0} - 40$	$T_{L\phi_0} - 40$	$T_{L\phi_0} - 40$	$T_{L\phi_0} - 40$	$T_{L\phi_0} - 10$	ns
Delay Between $\phi_1$ and $\phi_2$	$T_D$	5	—	5	—	5	—	5	—	ns
$\phi_1$ and $\phi_2$ Rise and Fall Times <sup>(1,3)</sup>	$T_R, T_F$	—	25	—	25	—	15	—	15	ns
<b>UM6502E</b>										
R/W Setup Time	$T_{RWS}$	—	125	—	100	—	75	—	60	ns
R/W Hold Time	$T_{RWH}$	30	—	30	—	15	—	15	—	ns
Address Setup Time	$T_{ADS}$	—	125	—	100	—	75	—	70	ns
Address Hold Time	$T_{ADH}$	30	—	30	—	15	—	15	—	ns
Read Access Time	$T_{ACC}$	—	1000-225	—	500-150	—	330-115	—	250-105	ns
Read Data Setup Time	$T_{DSU}$	100	—	50	—	40	—	35	—	ns
Read Data Hold Time	$T_{HR}$	10	—	10	—	10	—	10	—	ns
Write Data Setup Time	$T_{MDS}$	20	175	—	100	—	75	—	60	ns
Write Data Hold Time	$T_{HW}$	60	—	60	—	30	—	30	—	ns
Sync Setup Time	$T_{SYS}$	—	125	—	100	—	75	—	60	ns
Sync Hold Time	$T_{SYH}$	30	—	30	—	15	—	15	—	ns
RDY Setup Time <sup>(4)</sup>	$T_{RS}$	200	—	150	—	120	—	120	—	ns
<b>UM6512</b>										
Cycle Time	$T_{CYC}$	1.00	40	0.50	40	0.33	40	0.25	40	$\mu\text{s}$
$\phi_1$ Pulse Width	$T_{PWH\phi_1}$	430	—	215	—	150	—	—	—	ns
$\phi_2$ Pulse Width	$T_{PWH\phi_2}$	470	—	235	—	160	—	—	—	ns
Delay Between $\phi_1$ and $\phi_2$	$T_D$	0	—	0	—	0	—	—	—	ns
$\phi_1$ and $\phi_2$ Rise and Fall Times <sup>(1)</sup>	$T_R, T_F$	0	25	0	20	0	15	—	—	ns

(Cont.)



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Parameter	Symbol	1 MHz		2 MHz		3 MHz		4 MHz		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
<b>UM6502/UM6507</b>										
Cycle Time	T <sub>CYC</sub>	1.00	40	0.50	40	0.33	40	0.25	40	μs
φ <sub>1</sub> (IN) Low Time <sup>(2)</sup>	T <sub>Lφ<sub>1</sub></sub>	480	—	240	—	160	—	110	—	ns
φ <sub>0</sub> (IN) High Time <sup>(2)</sup>	T <sub>Hφ<sub>0</sub></sub>	460	—	240	—	160	—	115	—	ns
φ <sub>0</sub> Neg to φ <sub>1</sub> Pos Delay <sup>(5)</sup>	T <sub>O1+</sub>	10	70	10	70	10	70	10	70	ns
φ <sub>0</sub> Neg to φ <sub>2</sub> Neg Delay <sup>(5)</sup>	T <sub>O2-</sub>	5	65	5	65	5	65	5	65	ns
φ <sub>0</sub> Pos to φ <sub>1</sub> Neg Delay <sup>(5)</sup>	T <sub>O1-</sub>	5	65	5	65	5	65	5	65	ns
φ <sub>0</sub> Pos to φ <sub>2</sub> Pos Delay <sup>(5)</sup>	T <sub>O2+</sub>	15	75	15	75	15	75	15	75	ns
φ <sub>0</sub> (IN) Rise and Fall Time <sup>(1)</sup>	T <sub>RO</sub> , T <sub>FO</sub>	0	30	0	20	0	15	0	10	ns
φ <sub>1</sub> (OUT), Pulse Width	T <sub>PWHφ<sub>1</sub></sub>	T <sub>Lφ<sub>0</sub></sub> -20	T <sub>Lφ<sub>0</sub></sub>	T <sub>Lφ<sub>0</sub></sub> -20	T <sub>Lφ<sub>0</sub></sub>	T <sub>Lφ<sub>0</sub></sub> -20	T <sub>Lφ<sub>0</sub></sub>	T <sub>Lφ<sub>0</sub></sub> -20	T <sub>Lφ<sub>0</sub></sub>	ns
φ <sub>2</sub> (OUT), Pulse Width	T <sub>PWHφ<sub>2</sub></sub>	T <sub>Lφ<sub>0</sub></sub> -40	T <sub>Lφ<sub>0</sub></sub> -10	T <sub>Lφ<sub>0</sub></sub> -40	T <sub>Lφ<sub>0</sub></sub> -40	T <sub>Lφ<sub>0</sub></sub> -40	T <sub>Lφ<sub>0</sub></sub> -10	T <sub>Lφ<sub>0</sub></sub> -40	T <sub>Lφ<sub>0</sub></sub> -10	ns
Delay Between φ <sub>1</sub> and φ <sub>2</sub>	T <sub>D</sub>	5	—	5	—	5	—	5	—	ns
φ <sub>1</sub> and φ <sub>2</sub> Rise and Fall Times <sup>(1, 3)</sup>	T <sub>R</sub> , T <sub>F</sub>	—	25	—	25	—	15	—	15	ns
<b>UM6502/UM6507/UM6512</b>										
R/W Setup Time	T <sub>RWS</sub>	—	225	—	140	—	110	—	90	ns
R/W Hold Time	T <sub>RWH</sub>	30	—	30	—	15	—	10	—	ns
Address Setup Time	T <sub>ADS</sub>	—	225	—	140	—	110	—	90	ns
Address Hold Time	T <sub>ADH</sub>	30	—	30	—	15	—	10	—	ns
Read Access Time	T <sub>ACC</sub>	—	650	—	310	—	170	—	110	ns
Read Data Setup Time	T <sub>DSU</sub>	100	—	50	—	50	—	50	—	ns
Read Data Hold Time	T <sub>HR</sub>	10	—	10	—	10	—	10	—	ns
Write Data Setup Time	T <sub>MDS</sub>	20	175	20	100	20	75	—	70	ns
Write Data Hold Time	T <sub>HW</sub>	60	150	60	150	30	130	20	—	ns
Sync Setup Time	T <sub>SYS</sub>	—	350	—	175	—	100	—	90	ns
Sync Hold Time	T <sub>SYH</sub>	30	—	30	—	15	—	15	—	ns
RDY Setup Time <sup>(4)</sup>	T <sub>RS</sub>	200	—	200	—	150	—	120	—	ns

Microprocessor

**Notes:**

1. Measured between 10% and 90% points.
2. Measured at 50% points.
3. Load = 1 TTL load + 30 pF.
4. RDY must never switch states within T<sub>RS</sub> to end of φ<sub>1</sub>.
5. Load = 100 pF.
6. The 2 MHz devices are identified by an "A" suffix.
7. The 3 MHz devices are identified by an "B" suffix.
8. The 4 MHz devices are identified by an "C" suffix.

**Timing Diagram Note:**

Because the clock generation for the UM6502/UM6502E/UM6507 and UM6512 is different, the two clock timing sections are referenced to the main timing diagram by three reference lines marked REF 'A', REF 'B' and REF 'C'. Reference between the two sets of clock timings is without meaning. Timing parameters referring to these lines and scale variations in the diagrams are of no consequence.



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## PIN FUNCTIONS

### Clocks ( $\phi_1$ , $\phi_2$ )

The UM6512 requires a two phase non-overlapping clock that runs at the  $V_{CC}$  voltage level.

The UM6502/UM6502E/UM6507 clocks are supplied with an internal clock generator. The frequency of these clocks is externally controlled. Clock generator circuits are shown elsewhere in this data sheet.

### Address Bus (AB0-AB15)

(See sections on each microprocessor for respective address lines on those devices.)

These outputs are TTL compatible, capable of driving one standard TTL load and 130 pF.

### Data Bus (DB0-DB7)

Eight pins are used for the data bus. This is a bi-directional bus, transferring data to and from the device and peripherals. The outputs are three-state buffers, capable of driving one standard TTL load and 130 pF.

### Data Bus Enable (DBE)

This TTL compatible input allows external control of the three-state data output buffers and will enable the microprocessor bus driver when in the high state. In normal operation DBE would be driven by the phase two ( $\phi_2$ ) clock, thus allowing data output from microprocessor only during  $\phi_2$ . During the read cycle, the data bus drivers are internally disabled, becoming essentially an open circuit. To disable data bus drivers externally, DBE should be held low. This signal is available on the UM6512 only.

### Ready (RDY)

This input signal allows the user to halt the microprocessor on all cycles except write cycles. A negative transition to the low state during or coincident with phase one, ( $\phi_1$ ) will halt the microprocessor with the output address lines reflecting the current address being fetched. This condition will remain through a subsequent phase two ( $\phi_2$ ) in which the Ready signal is low. This feature allows microprocessor interfacing with low speed PROMS as well as fast (max. 2 cycle) Direct Memory Access (DMA). If ready is low during a write cycle, it is ignored until the following read operation. Ready transitions must not be permitted during  $\phi_2$  time.

### Interrupt Request ( $\overline{IRQ}$ )

This TTL level input requests that an interrupt sequence begin within the microprocessor. The microprocessor will complete the current instruction being executed before recognizing the request. At the time, the interrupt mask bit in the Status Code Register will be examined. If the interrupt mask flag is not set, the microprocessor will begin an interrupt sequence. The Program Counter and Processor Status Register are stored in the stack. The microprocessor will then set the interrupt mask flag high so that no further interrupts may occur. At the end of this cycle, the program counter low will be loaded from address FFFE, and program counter high from location FFFF, therefore transferring program control to the memory vector located at these addresses. The RDY signal must be in the high state for any interrupt to be recognized. A 3K $\Omega$

external resistor should be used for proper wire-OR operation.

### Non-Maskable Interrupt ( $\overline{NMI}$ )

A negative going transition on this input requests that a non-maskable interrupt sequence be generated within the microprocessor.

$\overline{NMI}$  is an unconditional interrupt. Following completion of the current instruction, the sequence of operations defined for  $\overline{IRQ}$  will be performed, regardless of the state interrupt mask flag. The vector addresses loaded into the program counter, low and high, are locations FFFA and FFFB respectively, thereby transferring program control to the memory vector located at these addresses. The instructions loaded at these locations cause the microprocessor to branch to a non-maskable interrupt routine in memory.

$\overline{NMI}$  also requires an external 3K $\Omega$  resistor to  $V_{CC}$  for proper wire-OR operations.

Inputs  $\overline{IRQ}$  and  $\overline{NMI}$  are hardware interrupts lines that are sampled during  $\phi_2$  (phase 2) and will begin the appropriate interrupt routine on the  $\phi_1$  (phase 1) following the completion of the current instruction.

### Set Overflow Flag (S. O.)

A NEGATIVE going edge on this input sets the overflow bit in the Status Code Register. This signal is sampled on the trailing edge of  $\phi_1$ .

### SYNC

This output line is provided to identify those cycles in which the microprocessor is doing an OP CODE fetch. The SYNC line goes high during  $\phi_1$  of an OP CODE fetch and stays high for the remainder of that cycle. If the RDY line is pulled low during the  $\phi_1$  clock pulse in which SYNC went high, the processor will stop in its current state and will remain in the state until the RDY line goes high. In this manner, the SYNC signal can be used to control RDY to cause single instruction execution.

### Reset ( $\overline{RES}$ )

This input is used to reset or start the microprocessor from a power down condition. During the time that this line is held low, writing to or from the microprocessor is inhibited. When a positive edge is detected on the input, the microprocessor will immediately begin the reset sequence.

After a system initialization time of six clock cycles, the mask interrupt flag will be set and the microprocessor will load the program counter from the memory vector locations FFFC and FFFD. This is the start location for program control.

After  $V_{CC}$  reaches 4.75 volts in a power up routine, reset must be held low for at least two clock cycles. At this time the R/ $\overline{W}$  and SYNC signal will become valid. When the reset signal goes high following these two clock cycles, the microprocessor will proceed with the normal reset procedure detailed above.

### Read/Write (R/ $\overline{W}$ )

This output signal is used to control the direction of data transfers between the processor and other circuits on the data bus. A high level on R/ $\overline{W}$  signifies data into the processor; a low is for the data transfer out of the processor.



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**PROGRAMMING CHARACTERISTICS**

**INSTRUCTION SET – ALPHABETIC SEQUENCE**

ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
BCC	Branch on Carry Clear	LSR	Shift One Bit Right (Memory or Accumulator)
BCS	Branch on Carry Set.	NOP	No Operation
BEQ	Branch on Result Zero	ORA	"OR" Memory with Accumulator
BIT	Test Bits in Memory with Accumulator	PHA	Push Accumulator on Stack
BMI	Branch on Result Minus	PHP	Push Processor Status on Stack
BNE	Branch on Result not Zero	PLA	Pull Accumulator from Stack
BPL	Branch on Result Plus	PLP	Pull Processor Status from Stack
BNK	Force Break	ROL	Rotate One Bit Left (Memory or Accumulator)
BVC	Branch on Overflow Clear	ROR	Rotate One Bit Right (Memory or Accumulator)
BVS	Branch on Overflow Set	RTI	Return from Interrupt
CLC	Clear Carry Flag	RTS	Return from Subroutine
CLD	Clear Decimal Mode	SBC	Subtract Memory from Accumulator with Borrow
CLI	Clear Interrupt Disable Bit	SEC	Set Carry Flag
CLV	Clear Overflow Flag	SED	Set Decimal Mode
CMP	Compare Memory and Accumulator	SEI	Set Interrupt Disable Status
CPX	Compare Memory and Index X	STA	Store Accumulator in Memory
CPY	Compare Memory and Index Y	STX	Store Index X in Memory
DEC	Decrement Memory by One	STY	Store Index Y in Memory
DEX	Decrement Index X by One	TAX	Transfer Accumulator to Index X
DEY	Decrement Index Y by One	TAY	Transfer Accumulator to Index Y
EOR	"Exclusive-or" Memory with Accumulator	TSX	Transfer Stack Pointer to Index X
INC	Increment Memory by One	TXA	Transfer Index X to Accumulator
INX	Increment Index X by One	TXS	Transfer Index X to Stack Pointer
INY	Increment Index Y by One	TYA	Transfer Index Y to Accumulator
JMP	Jump to New Location		
JSR	Jump to New Location Saving Return Address		

Microprocessor

**ADDRESSING MODES**

**Accumulator Addressing**

This form of addressing is represented with a one byte instruction, implying an operation on the accumulator.

**Immediate Addressing**

In immediate addressing, the operand is contained in the second byte of the instruction, with no further memory addressing required.

**Absolute Addressing**

In absolute addressing, the second byte of the instruction specifies the eight low order bits of the effective address while the third byte specifies the eight high order bits. Thus, the absolute addressing mode allows access to the entire 65K bytes of addressable memory.

**Zero Page Addressing**

The zero page instructions allow for shorter code and execution times by only fetching the second byte of the

instruction and assuming a zero high address byte. careful use of the zero page can result in significant increase in code efficiency.

**Indexed Zero Page Addressing – (X, Y indexing)**

This form of addressing is used in conjunction with the index register and is referred to as "Zero Page, X" or "Zero Page, Y." The effective address is calculated by adding the second byte to the contents of the index register. Since this is a form of "Zero Page" addressing, the content of the second byte references a location in page zero. Additionally due to the "Zero Page" addressing nature of this mode, no carry is added to the high order 8 bits of memory and crossing of page boundaries does not occur.

**Indexed Absolute Addressing – (X, Y indexing)**

This form of addressing is used in conjunction with X and Y index registers and is referred to as "Absolute,





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X," and "Absolute, Y." The effective address is formed by adding the contents of X or Y to the address contained in the second and third bytes of the instruction. This mode allows the index register to contain the index or count value and the instruction to contain the base address. This type of indexing allows any location referencing and the index to modify multiple fields resulting in reduced coding and execution time.

**Implied Addressing**

In the implied addressing mode, the address containing the operand is implicitly stated in the operation code of the instruction.

**Relative Addressing**

Relative addressing is used only with branch instructions and establishes a destination for the conditional branch.

The second byte of the instruction becomes the operand which is an "Offset" added to the contents of the lower eight bits of the program counter when the counter is set at the next instruction. The range of the offset is -128 to + 127 bytes from the next instruction.

**Indexed Indirect Addressing**

In indexed indirect addressing (referred to as [Indirect, X]), the second byte of the instruction is added to the contents of the X index register, discarding the carry.

The result of this addition points to a memory location on page zero whose content is the low order eight bits of the effective address. The next memory location in page zero contains the high order eight bits of the effective address. Both memory locations specifying the high and low order bytes of the effective address must be in page zero.

**Indirect Indexed Addressing**

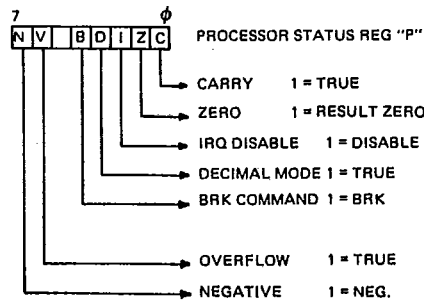
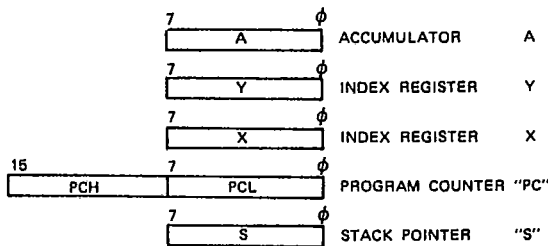
In indirect indexed addressing (referred to as [Indirect, Y]), the second byte of the instruction points to a memory location in page zero. The content of this memory location is added to the contents of the Y index register, the result being the low order eight bits of the effective address. The carry from this addition is added to the contents of the next page zero memory location, the result being the high order eight bits of the effective address.

**Absolute Indirect**

The second byte of the instruction contains the low order eight bits of a memory location. The high order eight bits of that memory location is contained in the third byte of the instruction. The content of the fully specified memory location is the low order byte of the effective address. The next memory location contains the high order byte of the effective address which is loaded into the sixteen bits of the program counter.

**PROGRAMMING CHARACTERISTICS**

**PROGRAMMING MODEL**







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Instruction Set

INSTRUCTIONS		IMME-DIATE			ABSO-LUTE			ZERO-PAGE			ACCUM			IMPLIED			(IND. X)			(IND. Y)				
MNEMONIC	OPERATION	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#		
A A A B B B	D N S C C C	C D L C S	A + M + C → A (4) (1) A ← M → A (1) C ← [7] 0 ← 0 BRANCH ON C = 0 (2) BRANCH ON C = 1 (2)	69 29	2 2	2 2	6D 2D 0E	4 4 6	3 3 3	65 25 06	3 3 5	2 2 2					61 21	6 6	2 2	71 31	6 5	2 2		
B B B B B	E I M N P	Q T I E L	BRANCH ON Z = 1 (2) A ← M BRANCH ON N = 1 (2) BRANCH ON Z = 0 (2) BRANCH ON N = 0 (2)				2C	4	3	24	3	2												
B B B C C	R V V L L	K C S C D	BREAK BRANCH ON V = 0 (2) BRANCH ON V = 1 (2) 0 → C 0 → D											00 18 D8	7 2 2	1 2 1								
C C C C C	L L M P P	I V P X Y	0 → I 0 → V A - M X - M Y - M	C9 E0 C0	2 2 2	2 2 2	CD EC CC	4 4 4	3 3 3	C5 E4 C4	3 3 3	2 2 2					C1	6	2	D1	5	2		
D D D E I	E E E Y R	C X Y R	M - 1 → M X - 1 → X Y - 1 → Y AVM → A (1) M + 1 → M	49	2	2	CE 4D EE	6 4 6	3 3 3	C6 45 E6	6 3 5	2 2 2		CA 88	2 2	1 1			41	6	2	51	5	2
I J J L S D R A	N M P P D R A	X Y R A	X + 1 → X Y + 1 → Y JUMP TO NEW LOC JUMP SUB M → A (1)	A9	2	2	4C 20 AD	3 6 4	3 3 3	A5	3	2		E8 C8	2 2	1 1			A1	6	2	B1	5	2
L L L N O R A	D D S O R P A	X Y R A	M → X (1) M → Y (1) 0 → [7] 0 → C NO OPERATION AVM → A	A2 A0	2 2	2 2	AE AC 4E	4 4 6	3 3 3	A6 A4 46	3 3 5	2 2 2	4A	2	1	EA	2	1	01	6	2	11	5	2
P P P P R O	H L L L P R O	A P A P L	A → MS S - 1 → S P → MS S - 1 → S S + 1 → S MS → A S + 1 → S MS → P ← [7] 0 ← [C] ←				2E	6	3	28	5	2	2A	2	1	48 08 68 28	3 3 4 4	1 2 1 1						
R R R R S S S E E D	O T T B S S E E D	R I S C C D	[C] → [0] 7 → 1 RTRN INT RTRN SUB A - M - C → A (1) 1 → C 1 → D	E9	2	2	6E ED	6 4	3 3	66 E5	6 3	2 2	6A	2	1	40 60 38 F8	6 6 2 2	1 1 1 1	E1	6	2	F1	5	2
S S S T T Y A X	E T T Y A X	I A X M Y X	1 → I A → M X → M Y → M A → X				8D 8E 8C	4 4 4	3 3 3	85 86 84	3 3 3	2 2 2		78 AA	2 2	1 1			81	6	2	91	6	2
T T T T Y A	A X X S A Y	A X A S Y	A → Y S → X X → A X → S Y → A											A8 BA 8A 9A 98	2 2 2 2 2	1 1 1 1 1								

- (1) ADD 1 TO N IF PAGE BOUNDARY IS CROSSED
- (2) ADD 1 TO N IF BRANCH OCCURS TO SAME PAGE  
ADD 2 TO N IF BRANCH OCCURS TO DIFFERENT PAGE
- (3) CARRY NOT = BORROW
- (4) IF IN DECIMAL MODE Z FLAG IS INVALID  
ACCUMULATOR MUST BE CHECKED FOR ZERO RESULT

T-49-17-06



UM6502E

Z PAGE. X			ABS. X			ABS. Y			RELATIVE			INDIRECT			Z PAGE. Y			PROCESSOR STATUS CODES								Mnemonic		
OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	7	6	5	4	3	2	1	0			
																		N	V	.	B	D	I	Z	C	Mnemonic		
76 35 16	4 4 6	2 2 2	7D 3D 1E	4 4 7	3 3 3	79 39	4 4	3 3										N	V	.	.	.	.	Z	C	A	D	C
									90 80	7 2	2 2							N	.	.	.	.	.	Z	C	A	D	C
									F0	2	2							M <sub>7</sub>	M <sub>6</sub>	.	.	.	.	Z	.	B	E	Q
									30 D0 10	2 2 2	2 2 2							.	.	.	.	.	.	.	B	E	Q	
									50 70	2 2	2 2							.	.	1	.	1	.	.	B	R	K	
																		.	.	.	.	.	0	.	B	R	K	
D6	4	2	DD	4	3	D9	4	3									N	0	.	.	.	.	0	.	C	L	I	
																		N	.	.	.	.	.	Z	C	L	V	
																		N	.	.	.	.	.	Z	C	L	P	
																		N	.	.	.	.	.	Z	C	L	X	
D8	6	2	DE	7	3													N	.	.	.	.	.	Z	.	D	E	C
55 F6	4 6	2 2	6D FE	4 7	3 3	69	4	3										N	.	.	.	.	.	Z	.	D	E	C
																		N	.	.	.	.	.	Z	.	D	E	C
												6C	5	3				N	.	.	.	.	.	Z	.	I	N	X
																		N	.	.	.	.	.	Z	.	I	N	X
85	4	2	8D	4	3	89	4	3										N	.	.	.	.	.	Z	.	I	N	X
																		N	.	.	.	.	.	Z	.	I	N	X
84 56 15	4 6 4	2 2 2	BC 5E 1D	4 7 4	3 3 3	BE	4	3							86	4	2	N	.	.	.	.	.	Z	.	L	D	X
																		N	.	.	.	.	.	Z	.	L	D	X
																		N	.	.	.	.	.	Z	.	L	D	X
																		N	.	.	.	.	.	Z	.	L	D	X
36	6	2	3E	7	3													N	.	.	.	.	.	Z	.	P	H	A
																		N	.	.	.	.	.	Z	.	P	H	A
																		N	.	.	.	.	.	Z	.	P	H	A
																		N	.	.	.	.	.	Z	.	P	H	A
76	6	2	7E	7	3													N	.	.	.	.	.	Z	.	R	O	R
																		N	.	.	.	.	.	Z	.	R	O	R
																		N	.	.	.	.	.	Z	.	R	O	R
																		N	.	.	.	.	.	Z	.	R	O	R
F5	4	2	FD	4	3	F9	4	3										N	V	.	.	.	.	Z	(3)	R	O	R
																		N	.	.	.	.	.	Z	1	R	O	R
																		N	.	.	.	.	.	Z	.	R	O	R
																		N	.	.	.	.	.	Z	.	R	O	R
95	4	2	9D	5	3	99	5	3										.	.	.	.	.	1	.	S	E	I	
																		.	.	.	.	.	.	.	.	S	E	I
94	4	2																N	.	.	.	.	.	Z	.	S	E	I
																		N	.	.	.	.	.	Z	.	S	E	I
																		N	.	.	.	.	.	Z	.	T	A	X
																		N	.	.	.	.	.	Z	.	T	A	X
																		N	.	.	.	.	.	Z	.	T	A	X

Microprocessor

X INDEX X                    + ADD                    M<sub>7</sub> MEMORY BIT 7  
 Y INDEX Y                    - SUBTRACT            M<sub>6</sub> MEMORY BIT 6  
 A ACCUMULATOR             ^ AND                    n NO. CYCLES  
 M MEMORY PER EFFECTIVE ADDRESS    V OR                    # NO. BYTES  
 M<sub>s</sub> MEMORY PER STACK POINTER        ∨ EXCLUSIVE OR

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