04
Atari Confidential
for Atari use only.

COMPANY CONFIDENTIAL

DEVICE NUMBER
C021859

REVISIONS			
DOC. REV.	DEVICE REV.	COMMENTS	DATE

	DATE
DRAFTED BY: ELAINE HADAD	8/18/83
SYSTEMS ENGINEERING: [signature]	8-18-83
LOGIC ENGINEERING: [signature]	8/18/83
C.A.D. ENGINEERING: [signature]	8/18/83
TEST ENGINEERING: Jeffrey Leong	8/19/83
ORIGINATING DIVISION	
DIVISION APPROVAL	

ATARI, INCORPORATED
275 GIBRALTAR DRIVE
SUNNYVALE, CA 94086

ATARI®
Semiconductor Group

DEVICE NAME
AMY 1

DOCUMENT NUMBER
D021859

PAGE 1 OF 57 PAGES

TABLE OF CONTENTS

Table of Contents (Cont'd)

TABLE OF ILLUSTRATIONS

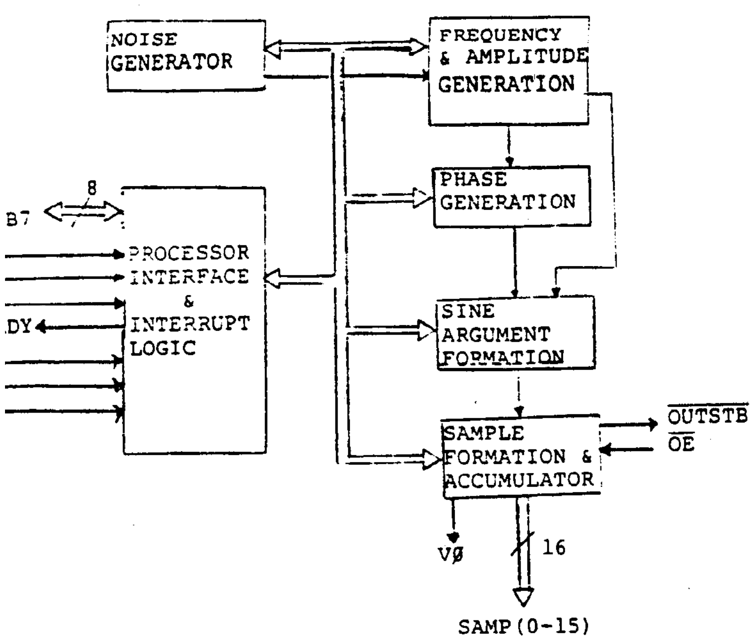
1. GENERAL DESCRIPTION

AMY 1 is a digital, pipeline architectured, additive music synthesizer chip. There are 8 voices maximum assignable with a total of 64 harmonic oscillators, available in groups of two, for voice assignment. AMY 1 has 72 independent, piecewise linear envelope generators: 8 fundamental frequency envelopes and 64 harmonic amplitude envelopes. A complete sound system requires addition of a D/A converter IC (up to 16 bit). To provide higher level commands, the system will generally include a controlling processor such as the Intel 8051 single chip microcomputer.

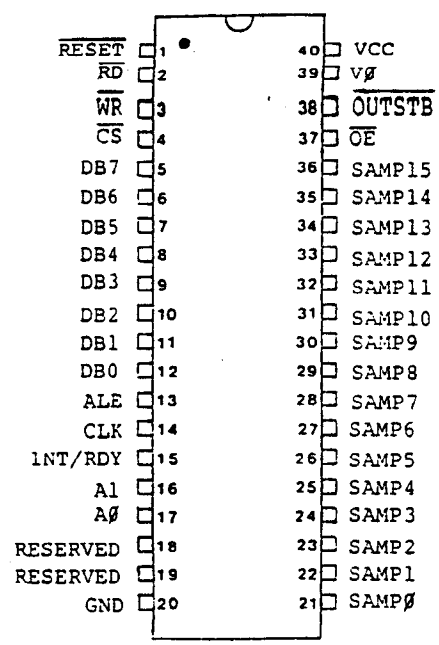
2. FEATURES

- o Single 40 pin DIP
- o 3u HMOS technology
- o Pipeline architecture
- o 10 MHz external clock frequency (maximum)
- o Integrated exponential ROM
- o 1/128 dB harmonic amplitude resolution & 1/64 semitone fundamental frequency resolution
- o Interrupt/Ready pin
- o Bus compatible with multiplexed and non-multiplexed bus microprocessors
- o Full 16 bit digital output width
- o Independent voice mode
- o Adjustable sample rate
- o Programmable noise statistics
- o 72 on chip envelope generators
- o Approximately 37,000 transistors

3. BLOCK DIAGRAM



4. PIN ASSIGNMENT



5. PIN DESCRIPTION

Pin Name	Type	Pin #	Function
V_{CC}	I	40	+5 volt supply (±5%).
GND	I	20	Ground.
$\overline{RESET}$	I	1	Reset. When low, performs a master reset on the AMY 1 chip. This signal asynchronously terminates device activity and clears the System Options register, System Control register, Sequencer, Control Counter, Subsample Counter, Phase RAM and Digital Output Word (SAMP bus).
A1-A0	I	16-17	Address lines. Used to select internal AMY 1 registers when not in ALE mode. A1 is the most significant bit. A1 and A0 should be tied to Ground when ALE mode is used.
$\overline{RD}$	I	2	Read strobe. Used to transfer contents of selected register onto the data bus line (DB0-DB7). $\overline{CS}$ pin must be low to enable the AMY bus drivers.
$\overline{WR}$	I	3	Write strobe. Used to load the selected AMY register from the data bus lines (DB0-DB7). $\overline{CS}$ must be low for the transfer to take place.
$\overline{CS}$	I	4	Chip select. When low, the $\overline{RD}$ and $\overline{WR}$ pins are enabled. When high, DB7-DB0 are tri-stated. The only time that AMY drives the data bus (DB7-DB0) is when $\overline{CS}$ = $\overline{RD}$ = 0.
CLK	I	14	10 MHz external clock (divided by 2 internally).
DB7-DB0	I/O	5-12	8 bit, tri-state data bus used to transfer data and commands between AMY 1 and the controlling CPU. DB7 is the most significant bit.

Pin Name	Type	Pin #	Function
SAMP15-SAMP0	O	36-21	16 bit data bus used to transfer data from AMY 1 to an external D/A converter. SAMP15 is the most significant bit. This bus is tri-stated unless the $\overline{OE}$ pin is low. This allows more than one device to share a single D/A converter.
$\overline{OUTSTB}$	O	38	Output strobe. When low, indicates that valid data is on the SAMP bus. (see Section 12.2).
INT/RDY	I	15	Interrupt/Ready. When operating in the READY mode, this pin is high only when AMY 1 is not executing a command. In the INTERRUPT mode, the pin generates a 1 clock period wide pulse when completing a command.
ALE	I	13	Address latch enable. When enabled, latches address information from the DB0 and DB1 bits of the data bus. The A0 and A1 pins are grounded when this pin is used. When not in use, ALE should be grounded.
V0	O	39	Voice zero. When operating in the INDIVIDUAL mode, the V0 pin will be high during one $\overline{OUTSTB}$ pulse per sample period. During this particular $\overline{OUTSTB}$ the data on the SAMP bus is the current sample for Voice 0.
$\overline{OE}$	I	37	Output enable. When low, the output SAMP data bus is enabled. When high, the output SAMP data bus is disabled.
RESERVED		18,19	Undefined.

6. FUNCTIONAL DESCRIPTION

6.1 Internal Architecture

AMY 1 consists of 8 major blocks as shown in Figure 1 below.

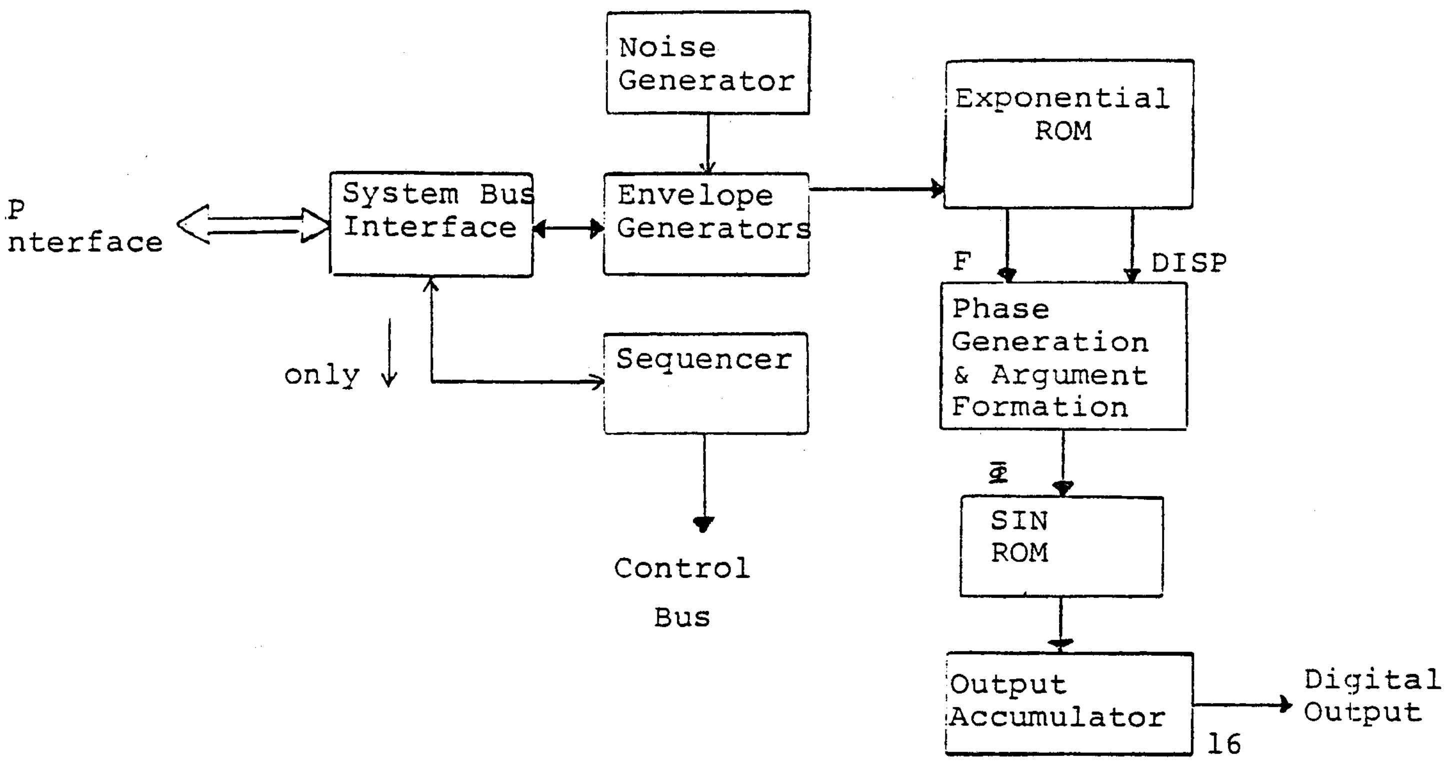


Figure 1. Simplified Block Diagram

The System Bus Interface block provides the user with a standard microprocessor interface. The user sends all commands and passes frequency and amplitude breakpoint data and current values over the "uP Interface" lines ($\overline{RESET}$, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, DB(0-7), ALE, INT/RDY, A1, A0).

The Noise Generator block contains a small RAM, a serial adder, and some associated logic. It generates two different channels of bandlimited white noise simultaneously. Bandwidths are programmable by initialization of the Noise RAM.

Internal Architecture (continued)

The Envelope Generator block contains the Voice RAM (VRAM), the Harmonic RAM (HRAM) and logic necessary to generate the 72 piecewise linear envelopes (8 fundamental frequency envelopes and 64 harmonic amplitude envelopes). The RAMs maintain a slope value, destination value and current value for each of the 72 envelopes (see Figure 2). The Voice RAM, in addition to slope, destination and current value, contains a 2 bit field for voice type selection. The total Envelope Generator RAM size is (64 x 29) + (21 x 16) bits = 278 bytes.

<u>HRAM Data Word Format</u>

13	8	8
Harmonic Amplitude Current Value	Harmonic Amplitude Destination	Harmonic Amplitude Slope

<u>VRAM Data Word Format</u>

13	8
Fundamental Frequency Destination	Fundamental Frequency Slope

and

18	2	1
Fundamental Frequency Current Value	Voice Type Select	Spare

Figure 2. HRAM and VRAM Data Word Format

Internal Architecture (continued)

The Envelope Generator block also contains the Last Harmonic Pair Flags (32) and an assortment of adders and other logic to generate all AMY envelopes from breakpoint information placed in the HRAM and VRAM by the sequencer under direction of the System Bus Interface command decoder. The Envelope Generator block also contains a Noise Adder. This is used in generating noise based voices.

The Exponential ROM converts the outputs of the 72 envelope generators to a piecewise exponential form for use internally. The ROM permits the AMY user to use decibel units for harmonic amplitude specification and semitone units for fundamental frequency specification. Not only are data widths reduced between the user and AMY, but master amplitude scaling and transposition operations are reduced to simple addition operations in the controlling processor.

The Sequencer block controls all the other blocks. It contains a 7 bit clock period counter and 7 bit subsample counter.

6.2 Complete AMY System

A complete sound system requires the addition of a D/A converter chip (up to 16 bit). To provide higher level commands the system will generally include a controlling processor such as the Intel 8051 Single Chip Microcomputer (see Figure 3 below).

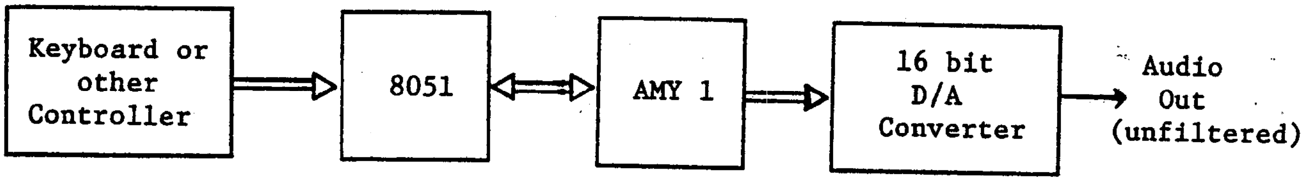


Figure 3. Complete AMY System Block

6.3 Envelope Generation

Envelopes are generated by the on chip AMY 1 envelope generator block. The user may command the generators to make any piecewise linear envelope desired by using a slope and destination scheme. Assume that a particular envelope generator has been previously loaded immediate to zero. By loading two breakpoints (slope-destination pairs) we can generate the following envelope:

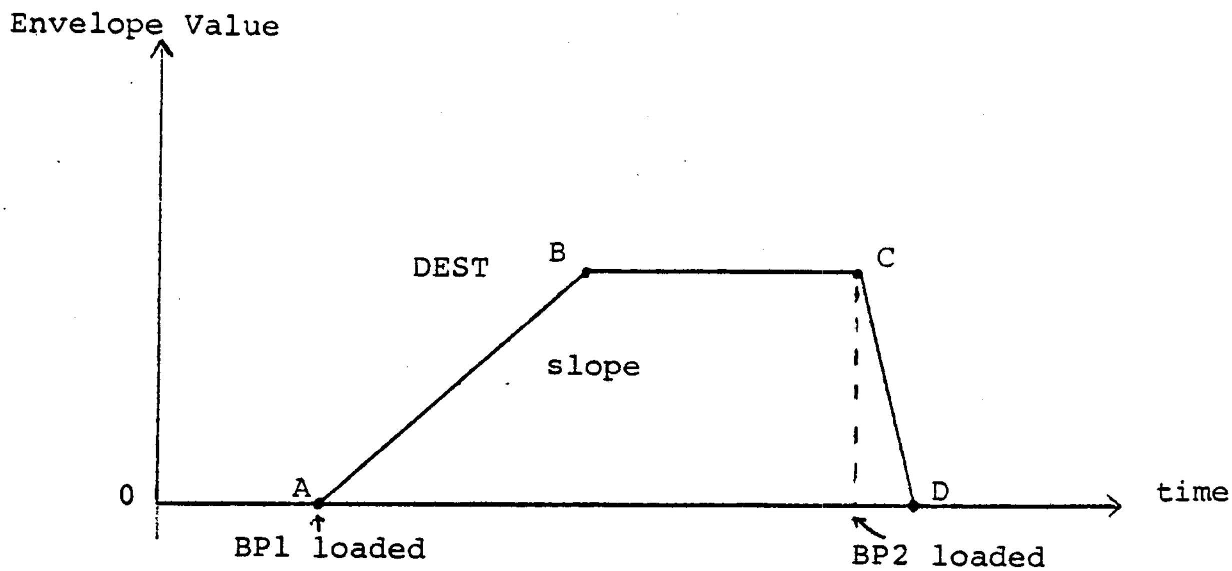


Figure 4. Piecewise linear envelope.

At Point A, BP1 is loaded and the envelope starts rising at a constant slope determined by the "slope" value of BP1. The envelope generator will continue to increase in value until the DEST value is reached. Point B is called a "Free point" since a change in slope has occurred without the user having to load another BP. At Point C, a BP with negative slope and DEST of zero has been loaded into AMY 1. The absolute value of the slope in BP2 is larger than that of BP1, and thus it takes less time for the envelope to "fall" than it did to "rise." Point D is another free point since when the DEST of zero is reached the envelope remains a zero (slope is effectively cleared when the destination is reached).

6.3.1 Slope Format

It is desirable to have a very wide range of slopes from nearly instantaneous changes in amplitude or pitch to nearly imperceptible changes in amplitude or pitch. To provide the AMY 1 user with an adequate range of slopes, an exponential format is used for all AMY 1 slopes. With this format, and also because all envelopes are exponentiated by the exponential ROM before use in the "oscillator" section of AMY 1, a tremendous dynamic range is accomplished (see Appendix II, Musical Specification). The AMY 1 slope format is:

sign bit	exponent		2's complement signed mantissa				
7	6	5	4	3	2	1	0

Each AMY 1 Harmonic Envelope Generator and Fundamental Frequency (pitch) Envelope Generator has its own slope byte. The sign bit determines whether the slope shall be positive or negative. The mantissa absolute value may range from 1 to 31 (or be 0). The exponent determines how often the mantissa is added (2's complement) to the current value of a particular envelope. If the exponent bits are both one (11), the envelope will be stepwise increased or decreased every other sample period. An exponent of "10" reduces the rate by a factor of 4 to every 8th sample period. An exponent of "01" reduces the rate by another factor of 4 to every 32nd envelope to be integrated only every 128 sample periods. Table 1 shows relative slopes for some sample slope bytes.

Slope	Byte						Relative Slope (steps/sample)
+/-	E1	E0	M4	M3	M2	M1	M0	
0	0	0	0	0	0	0	1	+1 step/128 sample periods = 7.8×10^{-3}
1	0	0	1	1	1	1	1	-1 step/128 sample periods = 7.8×10^{-3}
0	0	1	0	0	0	1	1	+3 steps/32 sample periods = 0.094
0	1	1	1	1	1	1	1	+31 steps/2 sample periods = 15.5
1	1	0	0	0	1	0	0	-28 steps/8 sample periods = -3.5
1	1	1	0	0	0	0	1	-31 steps/2 sample periods = -15.5

Table 1. Slope Examples

Notice that the ratio of the maximum to minimum slope is
$R = 15.5/7.8 \times 10^{-3} = 1984$

Slope Format (continued)

To achieve "smooth" pitch and amplitude modulation the "step" must be small. AMY 1 supports a pitch step of 1/2048 of a semitone (approximately a 0.0028% change in frequency) or, in music terms, 0.0488 cents. The amplitude step is 1/128 of a decibel. Both the pitch and amplitude steps were chosen so that pitch and amplitude envelopes will be sensed as "continuous" to the human ear for all AMY 1 slope values:

> Maximum Effective Amplitude Increement = ± 31/128 dB,
> Maximum Effective Fundamental Frequency Increment = ± 31/2048 semitones
> (Actual Fundamental Frequency Increment = ±1/64 semitones)

The harmonic envelope generators have a dynamic range of 64 dB, therefore, the total amplitude slope dynamic range is:

$$R * 10^{(\text{dB range}/20)} = 1984 * 10^{64\text{ dB}/20} = 3.2 * 10^{6} \text{ to } 1 \quad \text{(in volts/sec)}$$

The pitch (fundamental frequency) has a range of 10 2/3 octaves or 128 semitones. This implies a frequency slope dynamic range of:

$$R * 2^{(\text{octave range})} = 1984 * 2^{10.667} = 3.2 * 10^{6} \text{ to } 1 \quad \text{(in Hz/sec)}$$

* 1 cent = 1/100 semitone.

6.3.2 Destination Format

Since all harmonic amplitudes have a 64 dB dynamic range, a single 8 bit byte is used as a destination value for each harmonic amplitude. This leads to an amplitude destination resolution of:

$$\frac{64\ \text{dB}}{256} = 1/4\ \text{dB}$$

Harmonic Amplitude Destination Format and Examples

D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	Zero Amplitude
1	1	1	1	1	1	1	1	Full Scale (63.75 dB)
0	0	0	0	0	0	0	1	Minimum Harmonic Amplitude (0.25 dB)

The Harmonic Amplitude (dB) is a linear function of the Destination value.

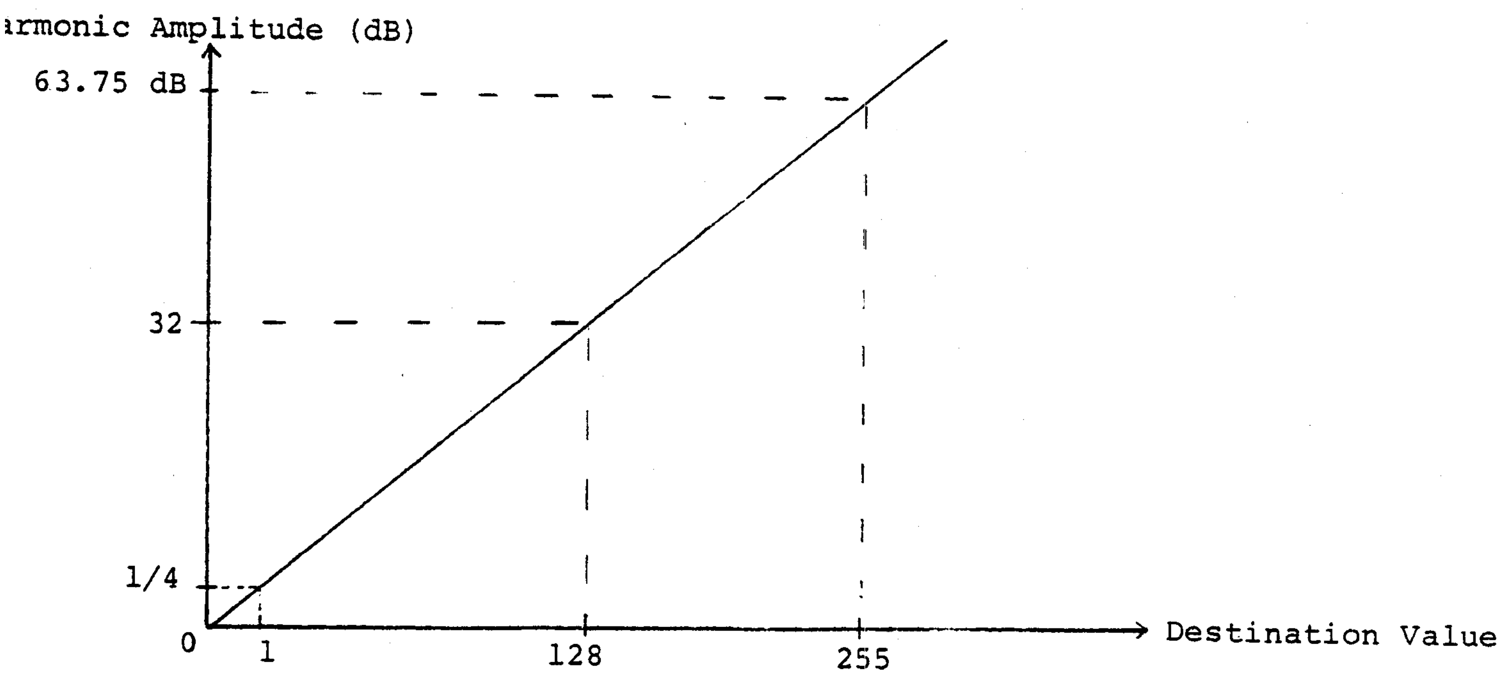


Figure 5. Linear Function of Harmonic Amplitude Destination.

Destination Format (continued)

Since all Fundamental Frequency envelope generators have a 128 semitone range and a frequency resolution of 1/64 semitones for the Destination is desirable, 13 bits are used in the Frequency destination word.

<u>Frequency Destination Format</u>

7	6
Semitone Field	ATARI Tone* Field

Again, the Fundamental Frequency (semitones) is a linear function of the Destination value.

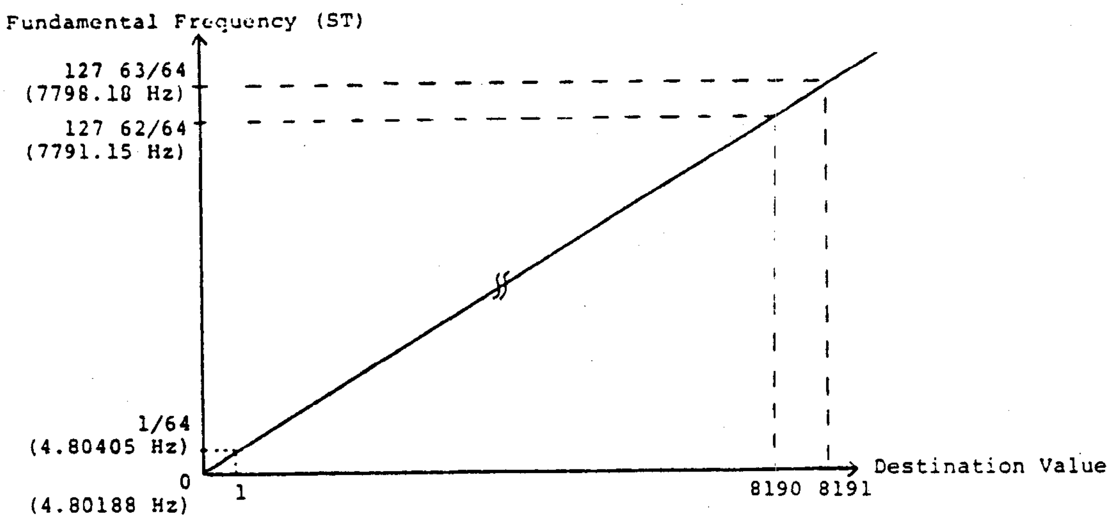


Figure 6. Fundamental Frequency vs. Destination.

Notice that a Destination value of 0000 Hex yields a non-zero frequency and that the frequency resolution around 0 is approximately 0.002 Hz per ATARI tone; at 8191 (or 1FFF Hex), the frequency resolution drops to approximately 7 Hz per ATARI tone. This is desirable and is made possible by the Exponential ROM.

Complete slope tables, computed for a 4 MHz internal clock rate using 64 harmonics, are included in Appendix I.

* 1 ATARI tone = 1/64 semitone

7. REGISTER ORGANIZATION

7.1 AMY 1 Command Set

A command may be sent to AMY 1 by setting $\overline{CS}$ = A1 = 0, $\overline{RD}$ = 1 and $\overline{WR}$ = 0. The command will be latched internally off the data bus on the trailing edge of the $\overline{WR}$ pulse. Each 8 bit command contains an opcode from 2 to 5 bits in length, and one or more operands (see Table 2 below).

DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Command
0	0	0	0	1	V2	V1	V0	Write Fundamental Frequency Breakpoint
0	0	0	1	0	V2	V1	V0	Write Voice Type
0	0	0	1	1	V2	V1	V0	Read Current Fundamental Frequency
0	0	1	0	SO3	SO2	SO1	SO0	Write System Options Register
0	0	1	1	X	X	SC1	SC0	Write System Control Register
0	1	H5	H4	H3	H2	H1	H0	Write Harmonic Amplitude Breakpoint
1	0	HP4	HP3	HP2	HP1	HP0	D0	Write Last Harmonic Pair Flag (Load SC1 bit = 0)
1	0	N5	N4	N3	N2	N1	N0	Write Noise RAM (Load SC1 bit = 1)
1	1	H5	H4	H3	H2	H1	H0	Read Current Harmonic Amplitude

Table 2. AMY 1 Commands

V2-V0: Voice Number
SO3-SO0: System Options register bits
SC1-SC0: System Control register bits
H5-H0: Harmonic Number
HP4-HP0: Harmonic Pair Number
N5-N0: Noise RAM location
X: Don't care

7.2 RAM and Register Areas

User access to internal RAM and register areas is through 4 registers: 3 data (Reg A (8 bits), Reg B (5 bits), Reg C (8 bits)) and one command register. Figure 7 shows all AMY 1 registers and RAM areas which are manipulated by the AMY 1 command set. To write to AMY 1 (e.g. "Write Fundamental Frequency Breakpoint" command), the user first sets up the proper values in the data registers A, B, and C, then issues the command to AMY 1's Command register.

When reading data from AMY 1 (e.g. "Read Current Fundamental Frequency" command), the user first writes the command to the Command register, then reads the value from the data registers.

Each of the 4 registers is read ($\overline{RD}$ = 0) or written ($\overline{WR}$ = 0) to through the data bus lines DB0-DB7 using a unique address on A0-A1 (see Table 3). In the case of a read from the Command register, AMY 1's internal bus will appear on DB0-DB7. This has no operational use and is provided for diagnostic purposes.

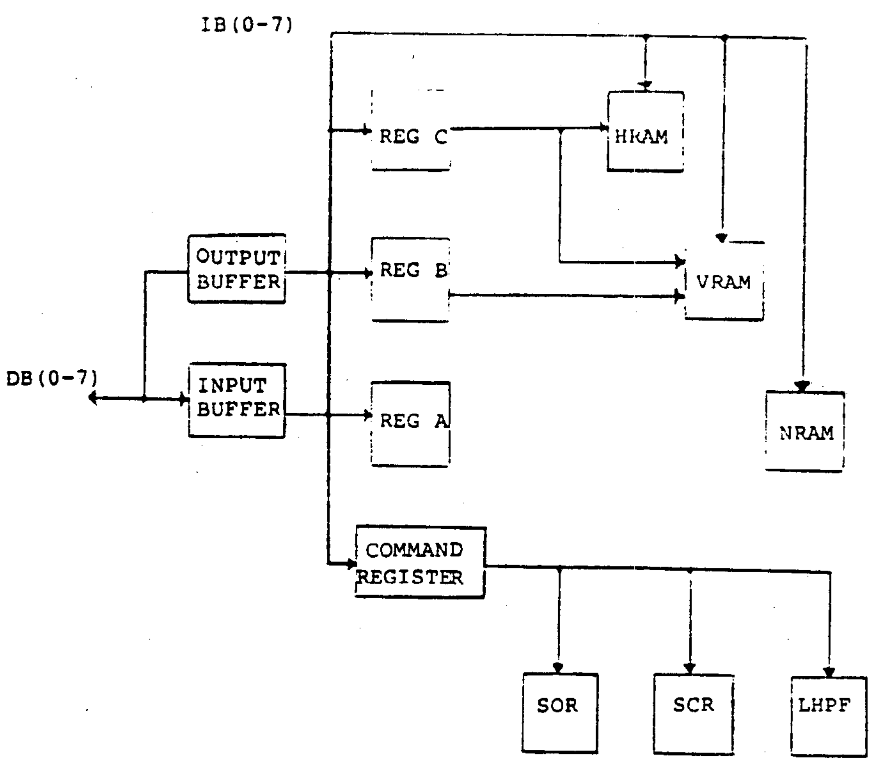


Figure 7. AMY RAM and Register Areas

7.3 AMY 1 Data Registers

There are 3 data registers for passing data between the user and AMY 1 internal RAM and Register storage areas. In general, the user loads the registers before sending a 'Write' command to AMY 1 (e.g. "Write Fundamental Frequency Breakpoint" command). Likewise, the user will read data from the registers after sending a 'Read' command to AMY 1 (e.g. "Read Current Fundamental Frequency" command). The registers are named Reg A, Reg B, and Reg C and are always directly accessible to the user since they have unique addresses (see Table 3).

$\overline{CS}$	A1	A0	Register Selected
0	0	0	Command (Write only)
0	0	1	Reg A
0	1	0	Reg B (Read or Write)
0	1	1	Reg C
1	X	X	None

Table 3. Register Selection.

Data bus lines DB0 through DB7 are used to pass all data between the user and the AMY 1 registers. DB0 through DB7 act as inputs (tri-state) unless $\overline{RD}$ = $\overline{CS}$ = 0, in which case the bus is driven by AMY 1 with the contents of the selected register. If the Command register is selected, the AMY 1 internal bus will be read.

7.4 Other User Accessible Registers and RAM Areas

AMY 1 also contains other internal registers which are loaded by sending various commands to the AMY 1 Command register. These registers are the System Options register, the System Control register, and the Last Harmonic Pair register (see Sections 7.5.5, 7.5.6, and 7.5.8, respectively).

Other AMY 1 commands pass data to or from AMY 1 RAM areas. These RAM areas include the Voice RAM, the Harmonic RAM, and the Noise RAM. The VRAM contains the current fundamental frequency, fundamental frequency breakpoint, and the voice type. The HRAM contains the current harmonic amplitude and the harmonic amplitude breakpoint. Initial conditions of the NRAM may be loaded to obtain specific bandlimited white noise statistics.

In general, all registers are loaded directly with a single one byte write operation (even the SOR, SCR, and LHPR are loaded from operand data in the command byte). Alternately, RAM areas are read/written to indirectly by using Reg A, B, and C as data buffers.

7.5 Command Descriptions

7.5.1 Write Fundamental Frequency Breakpoint Command (WR FFBP)

Command: | 0 | 0 | 0 | 0 | 1 | V2 | V1 | V0 |

This command loads a new fundamental frequency slope and destination (FFBP) for the desired voice into the voice RAM. This is done indirectly by loading Reg A, B, and C before the command is issued. V2, V1 and V0 are the voice pointer bits; that is, if V2 = V1 = V0 = 0, then Voice 0's FFBP (slope and destination) will be loaded. If V2 = V1 = 0 and V0 = 1, then Voice 1's FFBP will be modified. The register data format for this command is:

| B.4 – B.0 | ---------→ 5 MSB's of FF destination

| C.7 – C.0 | ---------→ 8 LSB's of FF destination

| A.7 – A.0 | ---------→ 8 bit slope

If the slope (Reg A) is zero when the Write FFBP command is issued, the destination will be loaded immediate into the FF current value field of the VRAM. It will remain there until another Write FFBP command is issued.

Write Fundamental Frequency Breakpoint (continued)

The slope and destination data are to be loaded into the A, B, and C registers before the WR FFBP command is executed.

Slope:

Register A:

A.7	A.6	A.5	A.4	A.3	A.2	A.1	A.0
Sign	Exponent		5 bit Mantissa				

Bits 7,4-0: Increment Value
(from -31/2048 to 31/2048 of a semitone)

A.7	A.4	A.3	A.2	A.1	A.0	Semitone Increment
0	1	1	1	1	1	31/2048
			.			.
			.			.
			.			.
0	0	0	0	1	0	2/2048
0	0	0	0	0	1	1/2048
0	0	0	0	0	0	Zero slope
1	1	1	1	1	1	-1/2048
1	1	1	1	1	0	-2/2048
			.			.
			.			.
			.			.
1	0	0	0	0	1	-31/2048
1	0	0	0	0	0	Not allowed

Bits 6-5: Subsample Rate Control

A.6	A.5	INCREMENT RATE
0	0	Add once every 128 sample periods
0	1	Add once every 32 sample periods
1	0	Add once every 8 sample periods
1	1	Add once every 2 sample periods

Destination:

There are 8196 possible destination values which cover a range of 128 semitones (1/64 of a semitone resolution).

7.5.2 Write Harmonic Amplitude Breakpoint Command (WR HABP)

Command:

0	1	H5	H4	H3	H2	H1	H0

This command loads a new Harmonic Amplitude slope and destination value (HABP) for the specified harmonic into the Harmonic RAM. The harmonic number is specified by the least significant 6 bits of the command byte (H5-H0). The operation is performed indirectly by loading Reg A and C before the command is issued. Reg B is not used in this command. The register format for this command is:

C.7	
-	---------→ 8 bit destination
C.0	

A.7	
-	---------→ 8 bit slope
A.0	

If the slope byte (Reg A) is zero when the command is issued, the destination will be loaded immediate into the HA current value field of the Harmonic RAM. It will remain at that value until another Write HABP command is issued. This mode is most useful in the "cold Start" software routine immediately after power up of AMY 1, since all harmonic amplitudes may be loaded immediate to zero before the SEQRUN bit is set (see Section 7.5.6).

Write Harmonic Amplitude Breakpoint Command (continued)

Slope:

Register A:

A.7	A.6	A.5	A.4	A.3	A.2	A.1	A.0
Sign	Exponent		5 bit Mantissa				

Bits 7,4-0: Increment Value
(from -31/128 to 31/128 of a decibel)

A.7	A.4	A.3	A.2	A.1	A.0	Increment (decibels)
0	1	1	1	1	1	31/128
			.			.
			.			.
			.			.
0	0	0	0	1	0	2/128
0	0	0	0	0	1	1/128
0	0	0	0	0	0	Zero Slope
1	1	1	1	1	1	-1/128
1	1	1	1	1	0	-2/128
			.			.
			.			.
			.			.
1	0	0	0	0	1	-31/128
1	0	0	0	0	0	Not allowed

Bits 6-5: Subsample Rate Control

A.6	A.5	Increment Rate
0	0	Add once every 128 sample periods
0	1	Add once every 32 sample periods
1	0	Add once every 8 sample periods
1	1	Add once every 2 sample periods

Destination:

There are 256 possible destination values covering a 64 dB dynamic range (1/4 of a decibel resolution).

7.5.3 Read Fundamental Frequency Current Value (RD FFCV)

Command:

0	0	0	1	1	V2	V1	V0

This command instructs the AMY 1 sequencer to read, from the Voice RAM, the current value field for the voice specified by the 3 LSB's of the command (V2, V1, V0) and load its contents into the B and C registers where it can be examined by the user. When reading Reg B, bits 7-5 are don't care. Reg A is not used in this command. The register format is as follows:

B.4 – B.0	----------> 5 MSB's of Current FF value
C.7 – C.0	----------> 8 LSB's of current FF value

7.5.4 Read Harmonic Amplitude Current Value (RD HACV)

Command:

1	1	H5	H4	H3	H2	H1	H0

This command instructs the AMY sequencer to read the current value of the harmonic (specified by the 6 LSB of the command byte) into Reg C. The user may then read Reg C for the current amplitude of the specified harmonic. The A and B registers are not used even though Reg B is modified by this command.

C.7 - C.0	---------> 8 bit Current Harmonic Amplitude Value

7.5.5 Write System Options Register (WR SOR)

Command:

0	0	1	0	S03	S02	S01	S00

This command allows the user to select 4 options in AMY 1 operation. The 4 options bits, described below, are loaded directly from the least significant 4 bits of the command byte. Reg A, B, and C are not used in this command. When RESET, bits S03-S00 default to zero.

S03 ---->	40/$\overline{\text{64}}$ Harmonics	Selects 40 or 64 HARMONICS
S02 ---->	$\overline{\text{SUM MODE}}$	Selects INDIVIDUAL voice output or SUM of all voices output format
S01 ---->	INT MODE	Select INTERRUPT or READY mode
S00 ---->	ALE MODE	Select ALE mode or ADDRESS pin mode

S03	S02	S01	S00	AMY Mode
X	X	X	0	ADDRESS PIN Mode
X	X	X	1	ALE Mode
X	X	0	X	READY Mode
X	X	1	X	INTERRUPT Mode
X	0	X	X	SUM Mode
X	1	X	X	INDIVIDUAL Mode
0	X	X	X	64 HARMONICS Mode
1	X	X	X	40 HARMONICS Mode
0	0	0	0	RESET State - Initialize Default (ADR pin, READY, SUM and 64 HARMONICS)

Table 4. System Options Register Selection.

Notes:

1. In ADDRESS PIN mode, Table 4 shows how register selection is accomplished by using the A1 and A0 pins.

2. In ALE mode, the user must put the address information on the data bus (DB1 and DB0) during the ALE strobe time. In multiplexed bus processors, like the 8051, this occurs shortly before the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ strobe times.)

7.5.6 Write System Control Register (WR SCR)

Command:

0	0	1	1	X	X	SC1	SC0

This command allows the user to stop the AMY 1 output accumulation process thus holding the output bus to zero, avoiding power up glitches. It also allows the user to place AMY 1 in a special "noise initialize mode." When the WR SCR command is sent, the least significant 2 bits of the command byte are loaded into the SCR. Reg A, B, and C are not used in this command. When RESET, bits SC1-SC0 default to zero.

SC1 ---->	NZINIT	Select Noise RAM mode or Last Harmonic Pair mode
SC0 ---->	SEQRUN	Software Reset

SC1	SC0	AMY Mode
X	0	HALT Mode
X	1	SEQUENCER RUN Mode
1	X	Initialize Noise RAM
0	X	NOISE RUN Mode

Table 5. System Control Register Selection.

Notes:

1. The Sequencer must be running to generate digital sound on the SAMP bus. (In HALT mode, if $\overline{OE}$ = "0", SAMP (14-0) = "0", SAMP15 = "1")

2. In HALT mode, AMY 1 resets the phase of all harmonic oscillators to zero (for selected voices only).

3. Initialization of the Noise RAM may be done in the HALT or the SEQUENCER RUN mode.

4. When in NOISE RUN mode, both Noise Generators are running and may be selected for use in a particular "Noise Voice" (see Write Voice Type command, Section 7.5.9).

7.5.7 Write Noise RAM Command

Command:

1	0	N5	N4	N3	N2	N1	N0

Note: To use this command, the NZINIT bit in the SCR must be set.

This command loads data from Reg A into the Noise RAM. The address of the Noise RAM is specified in the least significant 6 bits of the command byte. Valid Noise RAM addresses range from 00 to 1D Hex (Noise Generator 0) and from 28 to 3F Hex (Noise Generator 1). The Noise RAM takes up a total of 54 address locations. Loading Noise RAM data to addresses between 1E and 27 Hex is not recommended. Each of the 54 valid Noise RAM locations may be loaded with a 3 bit value. The value is specified by the least significant 3 bits of Reg A. Reg A must be loaded with the proper data before the WR Noise RAM command is issued. See Section 8.2 for the Initialization Flow Chart.

Reg A	
A.7	
A.6	
A.5	---------> 5 MSB's of Reg A are ignored
A.4	
A.3	
A.2 - A.0	---------> 3 bits of Noise RAM data

Write Noise RAM Command (continued)

Noise RAM Initialization Format

RAM Address MSB's	RAM Address LSB					
	0			1		
0 0 0 0 0	PRBA0	PRBB0	PRBC0	PRBA'0	PRBB'0	PRBC'0
0 0 0 0 1	PRBA1	PRBB1	PRBC1	PRBA'1	PRBB'1	PRBC'1
0 0 0 1 0	PRBA2	PRBB2	PRBC2	PRBA'2	PRBB'2	PRBC'2
0 0 0 1 1	PRBA3	PRBB3	PRBC3	PRBA'3	PRBB'3	PRBC'3
0 0 1 0 0	PRBA4	PRBB4	PRBC4	PRBA'4	PRBB'4	PRBC'4
0 0 1 0 1	PRBA5	PRBB5	PRBC5	PRBA'5	PRBB'5	PRBC'5
0 0 1 1 0	PRBA6	PRBB6	PRBC6	PRBA'6	PRBB'6	PRBC'6
0 0 1 1 1	PRBA7	PRBB7	PRBC7	PRBA'7	PRBB'7	PRBC'7
0 1 0 0 0	PRBA8	PRBB8	PRBC8	PRBA'8	PRBB'8	PRBC'8
0 1 0 0 1	PRBA9	PRBB9	PRBC9	PRBA'9	PRBB'9	PRBC'9
0 1 0 1 0	PRBA10	PRBB10	PRBC10	PRBA'10	PRBB'10	PRBC'10
0 1 0 1 1	PRBA11	PRBB11	PRBC11	PRBA'11	PRBB'11	PRBC'11
0 1 1 0 0	PRBA12	PRBB12	PRBC12	PRBA'12	PRBB'12	PRBC'12
0 1 1 0 1	PRBA13	PRBB13	PRBC13	PRBA'13	PRBB'13	PRBC'13
0 1 1 1 0	PRBA14	PRBB14	PRBC14	PRBA'14	PRBB'14	PRBC'14
1 0 1 0 0	UD0	B0	X	UD'0	B'0	X
1 0 1 0 1	UD1	B1	X	UD'1	B'1	X
1 0 1 1 0	UD2	B2	X	UD'2	B'2	X
1 0 1 1 1	UD3	B3	X	UD'3	B'3	X
1 1 0 0 0	UD4	B4	X	UD'4	B'4	X
1 1 0 0 1	UD5	B5	X	UD'5	B'5	X
1 1 0 1 0	UD6	B6	X	UD'6	B'6	X
1 1 0 1 1	UD7	B7	X	UD'7	B'7	X
1 1 1 0 0	UD8	B8	X	UD'8	B'8	X
1 1 1 0 1	UD9	B9	X	UD'9	B'9	X
1 1 1 1 0	UD10	B10	X	UD'10	B'10	X
1 1 1 1 1	UD11	B11	X	UD'11	B'11	X

UD0-UD11: Up/Down Counter Bits
PRB0-PRB14: Pseudo Random Bits
B0-B11: Noise Value Bits
X: Don't Care

If the RAM address is even, Noise Generator 0 is being accessed. If the RAM address is odd, Noise Generator 1 is being accessed. The UD and B bits are default to zero on RESET. See the Operating Manual for actual noise values.

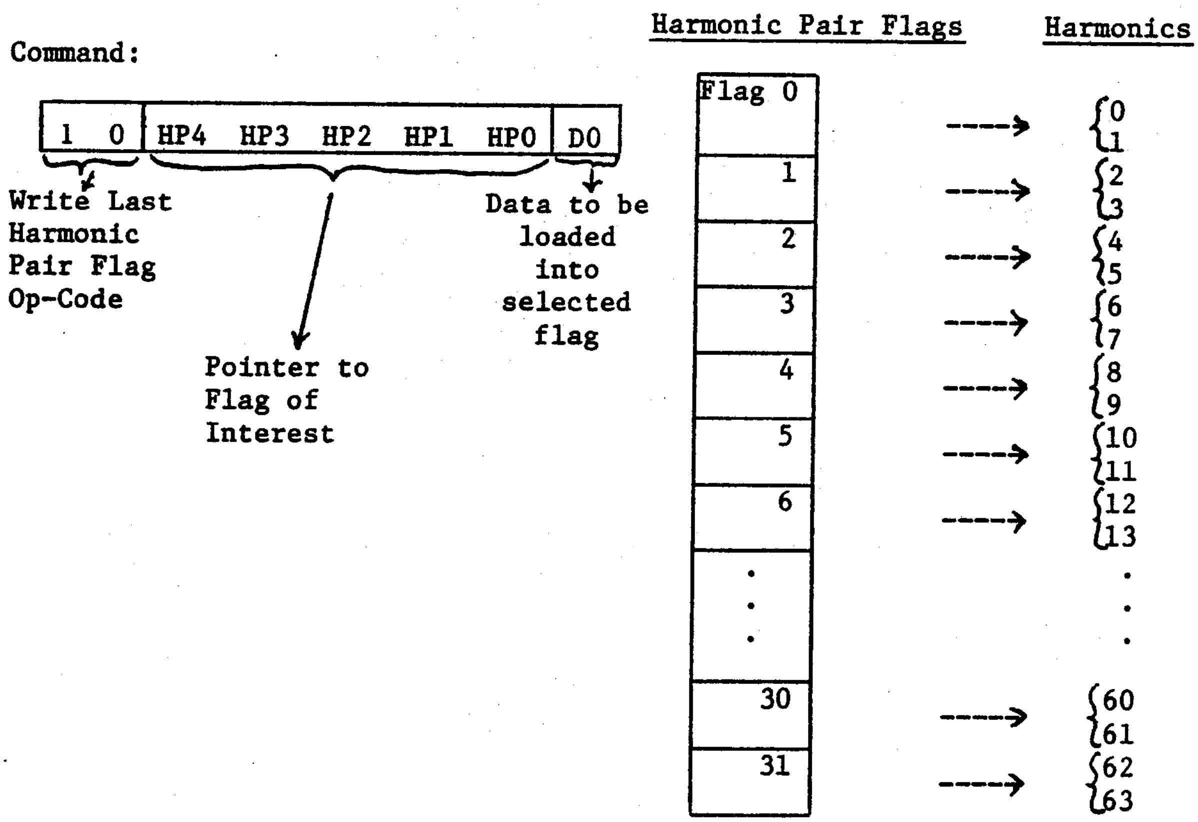
7.5.8 Write Last Harmonic Pair Flag Command

Command: `1  0  HP4  HP3  HP2  HP1  HP0  D0`

Note: To use this command, the NZINIT bit in the SCR must first be cleared.

This command allows the user to specify the number of harmonics allocated to each voice. There are a maximum of 8 voices and a maximum of either 40 or 64 harmonics (depending on the state of the 40/64 bit in the SOR). Harmonics must be allocated in groups of 2 or as harmonic pairs. Harmonics 0 and 1 are always assigned to Voice 0. Each pair of harmonics has a Last Harmonic Pair flag which determines whether or not these two harmonics are the last two harmonic of same voice. Therefore, there are 32 such flags. A maximum of 8 of these 32 flags should be set at any one time (since we are limited to 8 voices).

For a single voice of 64 harmonics, all last harmonic pair flags would be set to zero except the last one which is Last Harmonic Pair Flag 31. The HP4-HP0 field in the command byte specifies which flag is to be loaded. The LSB of the command byte (D0) specifies whether the flag is to be cleared or set. The 32 flags power up in a random state and thus all 32 must be set/cleared after power up to define the number of harmonics per voice. Reg A, B, and C are not used by this command.



Example: If all flags are reset except for Flag 3 = Flag 31 = 1, AMY 1 will be set up for 2 voices. Voice 0 will have 8 harmonics (0 through 7) and Voice 1 will have 56 harmonics (8 through 63).

7.5.9 Write Voice Type Command

Command:

0	0	0	1	0	V2	V1	V0

Each voice may be assigned as a Harmonic Voice or as one of two different Noise Source Based Voices. The desired voice is selected by the least significant 3 bits of the command byte. The least significant 2 bits of Reg A determine the "type" of voice desired. Reg A must be loaded before the command is issued according to the following convention (Reg B and C are not used):

```
A.7
 -    ---------> 6 MSB's unused
A.2
A.1   ---------> 2 LSB's determine voice type
A.0
```

A.1	A.0	Type
0	0	Harmonic
0	1	Noise Type 0
1	0	Noise Type 1
1	1	Illegal

8. OPERATING PROCEDURE

8.1 Initialization

8.1.1 RESET pin and Power up Sequence

Two milliseconds after power up, when spec power supply and clock requirements are met by the AMY 1 interface circuit, the $\overline{\text{RESET}}$ pin may be released (see Figure 8). Alternatively, 2 ms after power up (and before), the $\overline{\text{RESET}}$ pin must be held equal to or less than the V_{IL} spec for the $\overline{\text{RESET}}$ pin (see Figure 9).

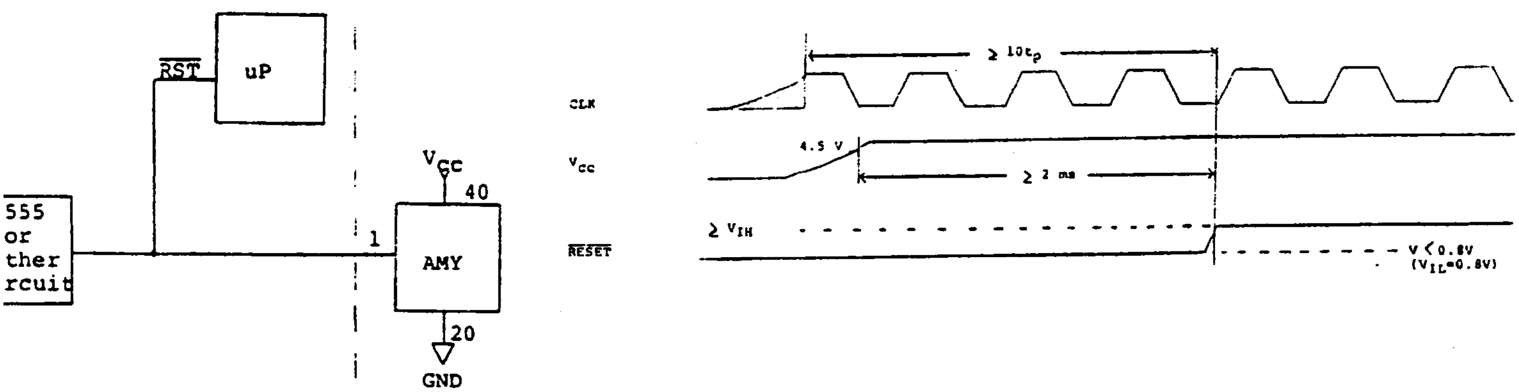
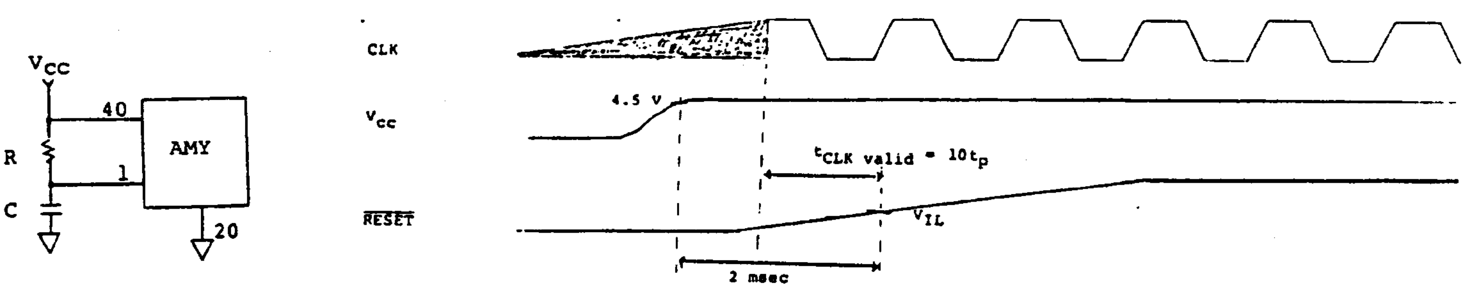


Figure 8. $\overline{\text{RESET}}$ with Standard Up System Reset Circuit

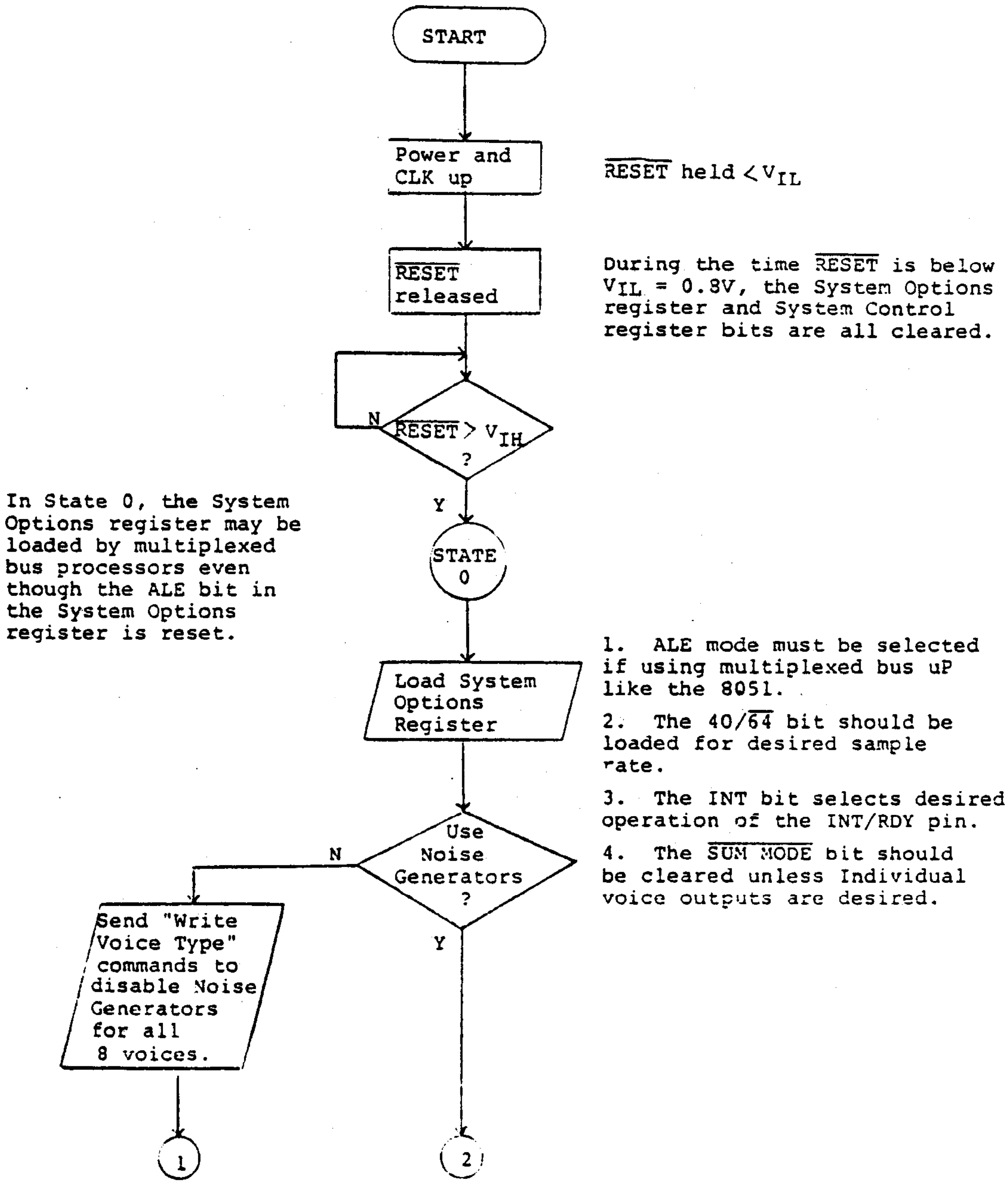


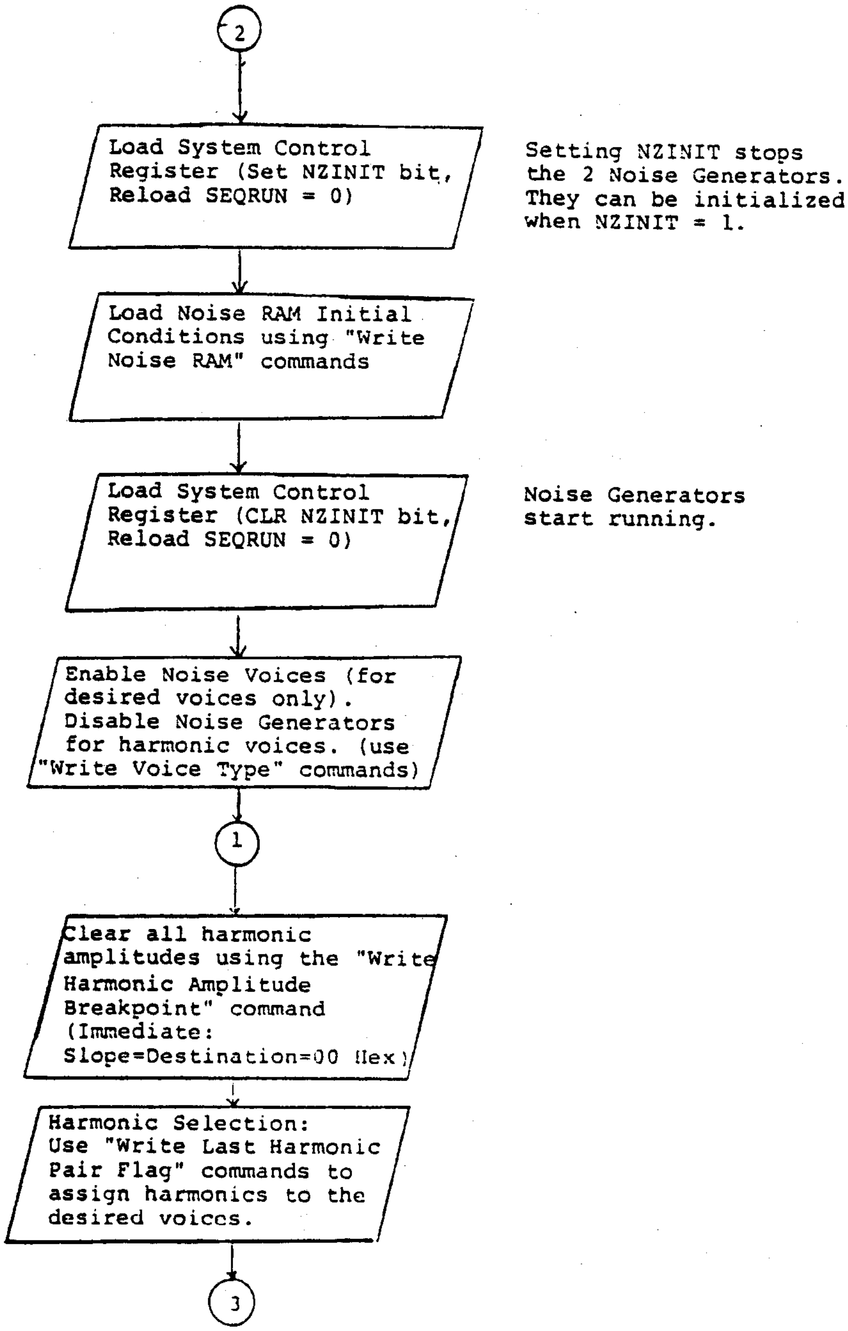
Note: RC requirements depend on V_{cc} rise time.

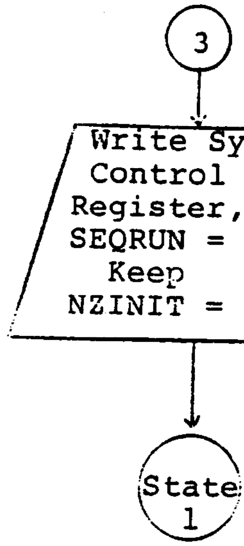
Figure 9. $\overline{\text{RESET}}$ with RC

8.2 Initialization Flow Chart

When RESET = 1, assuming the conditions of the previous page have been met, AMY 1 is in state 0 of the following chart:




2
Load System Control Register (Set NZINIT bit, Reload SEQRUN = 0)
Setting NZINIT stops the 2 Noise Generators. They can be initialized when NZINIT = 1.
Load Noise RAM Initial Conditions using "Write Noise RAM" commands
Load System Control Register (CLR NZINIT bit, Reload SEQRUN = 0)
Noise Generators start running.
Enable Noise Voices (for desired voices only). Disable Noise Generators for harmonic voices. (use "Write Voice Type" commands)
1
Clear all harmonic amplitudes using the "Write Harmonic Amplitude Breakpoint" command (Immediate: Slope=Destination=00 Hex)
Harmonic Selection: Use "Write Last Harmonic Pair Flag" commands to assign harmonics to the desired voices.
3



Although all oscillators are now running and the digital output bus (SAMP0-15) are no longer disabled, the SAMP bus will remain at the "Zero" level since all harmonic amplitudes have been loaded immediate to zero.

Run state

Once the user is in the RUN STATE (State 1), voices may be constructed by first loading the fundamental frequency immediate to some start value and then ramping up/down the Harmonic amplitudes (even the fundamental frequency, if desired). In State 1, an unlimited number of harmonic and fundamental frequency breakpoints may be loaded. Maximum bandwidth of breakpoints is approximately 200,000 BP/sec (essential for peaks in activity). Also, in State 1, the noise generators may be stopped and the Noise RAM reloaded (when the Noise Generator starts running again, the statistics of the noise may change). The number of harmonics per voice may also be modified. The user may change a voice's type, or may read current values of fundamental frequency for any voice or harmonic amplitude for any harmonic. When drastic changes are to be made it is recommended that the user return to State 0 by loading SEQRUN = 0 with the "Write System Control Register Command. In some cases, it may be desirable to "Ramp" all harmonic amplitudes to "zero" <u>before</u> loading SEQRUN = 0 (to avoid a "click").

8.3 Summary

Initialization of AMY 1 requires the following steps:

1. Loading System Options Register.

   a. Select 40 or 64 harmonics where the sample rate $= \frac{1}{2 * \# \text{ harmonics} * t_p}$, t_p = clock period

   Example: 64 harmonics with a 4 MHz internal clock rate results in a 31.25 KHz sample rate.

   b. Select ALE or Address Pin mode. If ALE mode is desired, the A0 and A1 pins should be tied to ground.

   c. Select INT/RDY pin function. If INT bit = 1, the INT/RDY pin will issue a single clock pulse wide interrupt pulse at the completion of all commands. If INT bit = 0, the INT/RDY pin will function as a Ready pin. In the READY mode, the INT/RDY pin will go low (logic 0) immediately upon receipt of a command and return high (logic 1) when the command has been completely executed (see Figure 10).

   d. Select between SUM mode (all voices added together and output once each sample period) or INDIVIDUAL mode (all voices output separately). There will be N output samples per sample period in the INDIVIDUAL mode- N is the number of voices enabled).

2. Defining voices using the "Write Last Harmonic Pair Flag" command.

3. Clearing all harmonic amplitudes to zero before setting SEQRUN = 1.

4. Loading initial conditions into Noise RAM using Write System Control register command and Write Noise RAM command.

5. Assigning each voice an initial voice type.

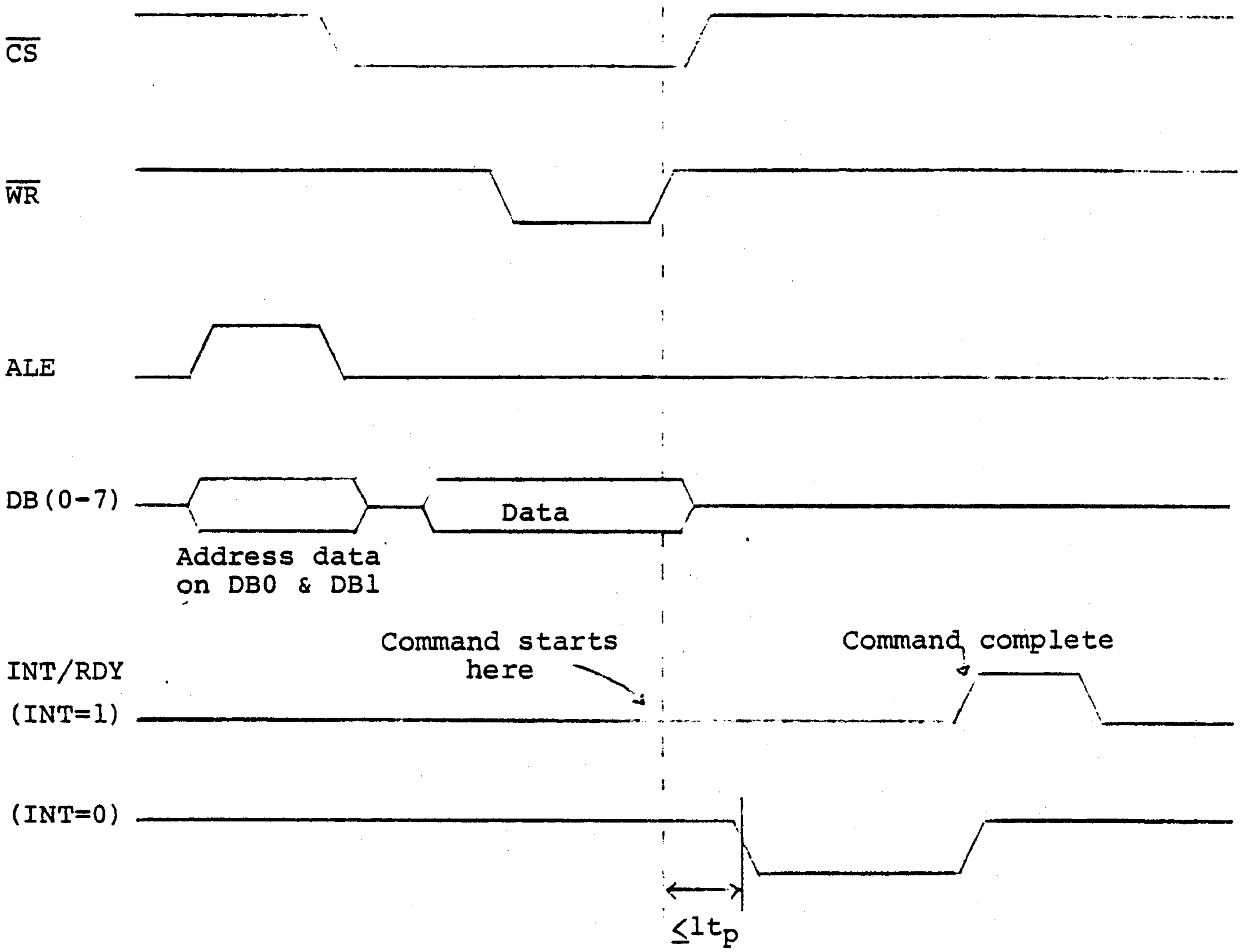


Figure 10. INT/RDY Pin Timing

9. MAXIMUM RATINGS beyond which useful life may be impaired

Storage Temperature	-65 to +150°C
Ambient Temperature Under Bias	0 to +70°C
Voltage at any Pin Relative to Ground	-0.5 to +7 V
Power Dissipation	1.0 W

10. CAPACITANCES

Ambient Temperature Parameters: T_A = 25°C; V_{cc} = GND = 0 V

Symbol	Parameter	Min	Max	Units	Test Conditions
C_{IN}	Input Capacitance		10	pF	
C_{OUT}	Output Capacitance		10	pF	

11. D.C. CHARACTERISTICS

Ambient Temperature Parameters: T_A = 0 to 70°C, V_{cc} = +5 V ± 5%

Symbol	Parameter	Min	Max	Units	Test Conditions
V_{IL}	Input Low Voltage	-0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	Vcc+0.5	V	
V_{OL}	Output Low Voltage		0.45	V	I_{OL} = 2 mA
V_{OH}	Output High Voltage	2.4		V	I_{OH} = -100uA
I_L	Input Leakage Current		10	uA	0 _ Vin _ 7.0 V
I_O	Output Leakage Current		10	uA	0.45_Vout_Vcc

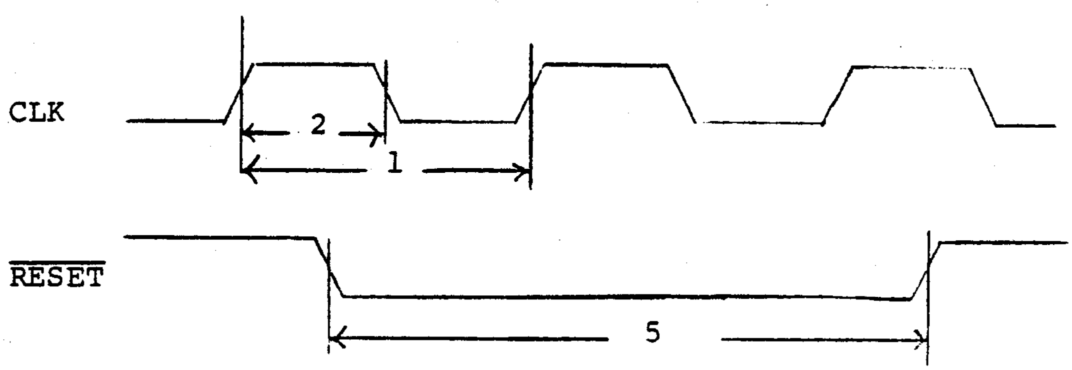
12. A.C. CHARACTERISTICS

12. CLOCK & RESET

T_A = 0 to 70°C
V_{cc} = 5 V ± 5%

Number	Symbol	Parameter	Min	Max	Unit	Comments
1	t_p	Clock Period	200	500	ns	
2	t_0	Clock High Time	$0.4t_p$	$0.6t_p$		
3	t_{cr}	Clock Rise Time		30	ns	10% to 90%
4	t_{cf}	Clock Fall Time		30	ns	10% to 90%
5	t_{rpw}	$\overline{\text{RESET}}$ Pulse Width	$2t_p$			

Note: RESET should be held low (less than V_{IL} = 0.8 Volts) during power up of the AMY 1 chip. It should remain low for greater than or equal to 2 msec after power meets spec (5 V ± 5%).

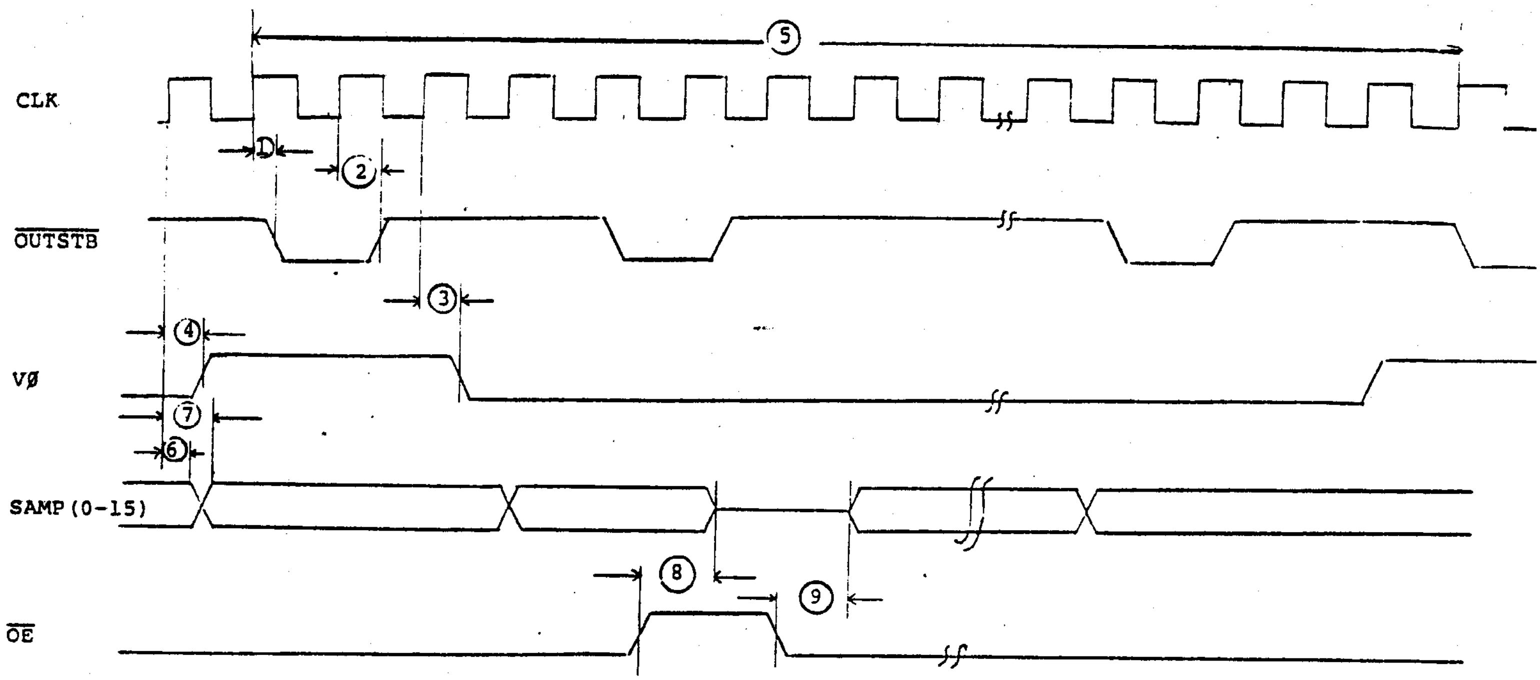


12.2 OUTPUT SECTION

T_A=0 to 70°C, C_L=150 pF unless noted

V_{cc}=5 V ±5%, 2 MHz_f_{clk}_5 MHz

Number	Symbol	Parameter	Min	Max	Unit	Comments
1	t_{col}	CLK to $\overline{OUTSTB}$ Low	Ø	150	nS	
2	t_{cot}	CLK to $\overline{OUTSTB}$ High	0	150	nS	
3	t_{cvt}	CLK to VO Falling Edge	0	150	nS	
4	t_{cvl}	CLK to VO Rising Edge	Ø	150	nS	
5	t_s	Sample Period				
		1) 40 Harmonic	$80t_p$	$80t_p$		t_p=1/f_{clk}
		2) 64 Harmonic	$128t_p$	$128t_p$		
6	t_{sh}	SAMP(0-15) Data Hold Time From CLK	20		nS	
7	t_{cshl}	CLK to SAMP(0-15) Data Valid		150	nS	OE_V_{IL}
8	t_{csf}	$\overline{OE}$ Rising Edge to SAMP(0-15) Output Float	0	150	nS	
9	t_{cse}	$\overline{OE}$ Falling to SAMP(0-15) Outputs Valid	0	150	nS	



Output Timing Diagram - Individual Mode

Notes:

1. VØ goes active one time (for several successive clock periods) each sample period.

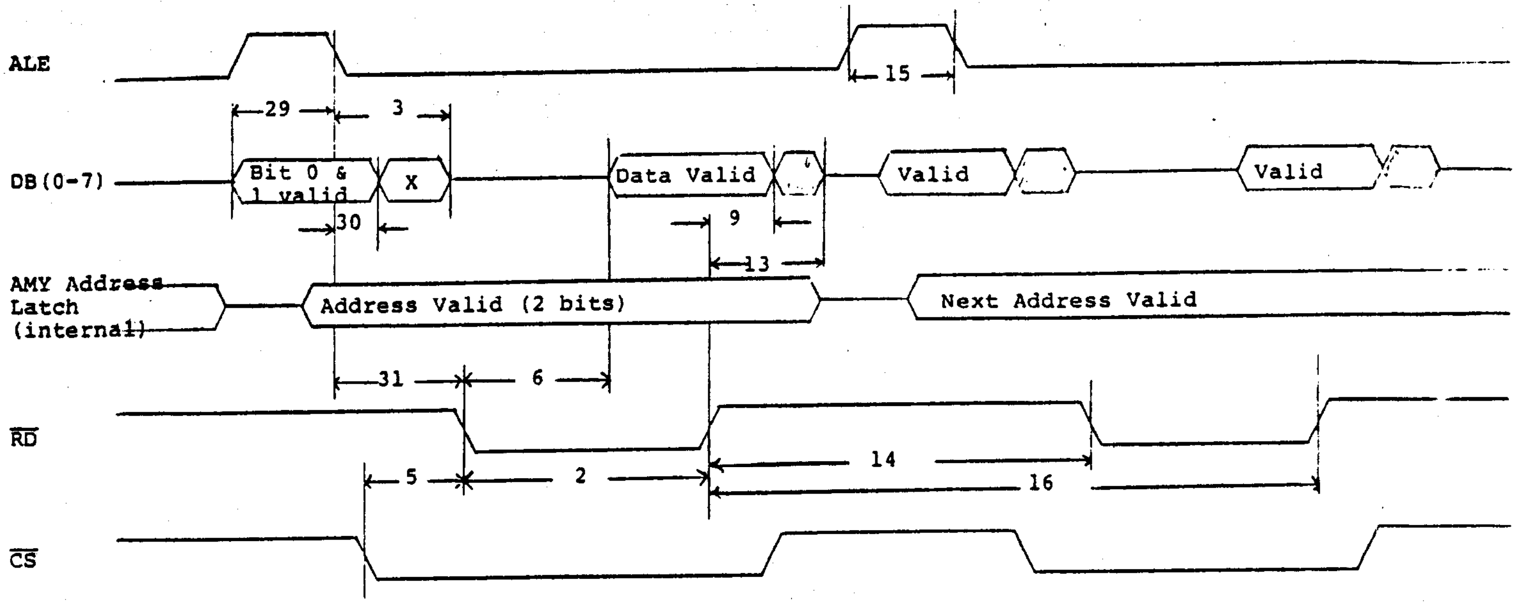
2. The number of OUTSTB pulses in one sample period is equal to the number of Voices in use. The time between OUTSTB pulses depends on the number of harmonics allocated to each voice. (ie, in the above diagram, Voice 1 has 2 harmonic oscillators assigned to it. - In general, if Voice N has 2 harmonics assigned to it, then Voice ((N-1) modulo M) samples are present on the samp bus for 2.2 clock periods (M = # Voice assigned).

12.3 SYSTEM BUS INTERFACE - Read Amy and Write Amy (Address Pin and ALE mode)

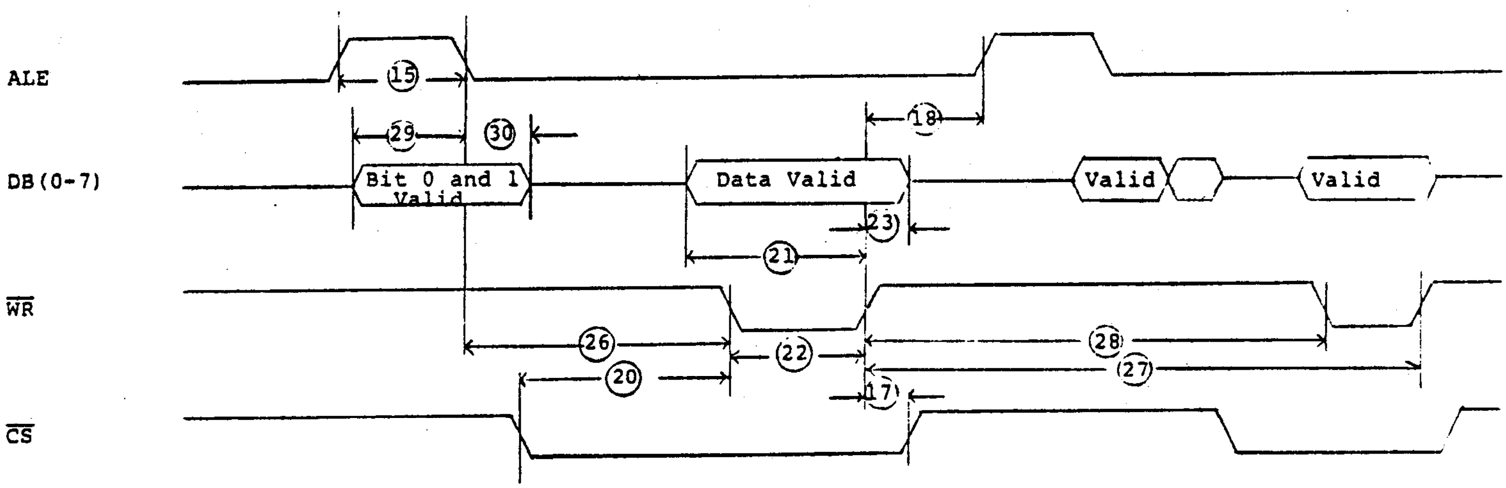
Number	Symbol	Parameter	Min	Max	Unit	Comments
1	t_{ar}	Address valid to $\overline{RD}$	0		nS	
2	t_{rr}	$\overline{RD}$ Pulse Width	200		nS	
3	t_{af}	ALE Float Time	10	100	nS	
4	t_{chr}	$\overline{CS}$ Hold Time after $\overline{RD}$	0		nS	
5	t_{cr}	$\overline{CS}$ Active to $\overline{RD}$	0		nS	
6	t_{rd}	Read Access Time	150		nS	
7	t_{ao}	Address to Data Valid	150		nS	
8	t_{cd}	$\overline{CS}$ Active to Data Valid	150		nS	
9	t_{rdh}	Data Bus Hold Time after $\overline{RD}$		10	nS	
10	t_{ahr}	Address Hold Time after $\overline{RD}$	0		nS	
11	t_{rdead1}	$\overline{RD}$ Dead Time (address pin mode)	100		nS	
12	t_{cycr1}	Read Cycle Time (address pin mode)	300		nS	
13	t_{rdf}	Read Float Time ($\overline{RD}$ to DB(0-7) Float)	10	100	nS	
14	t_{rdead2}	$\overline{RD}$ Dead Time (ALE Mode)	250		nS	
15	t_{apw}	ALE Pulse width	50		nS	
16	t_{cycr2}	ALE Mode Read Cycle Time	450		nS	

SYSTEM BUS INTERFACE (Cont.)

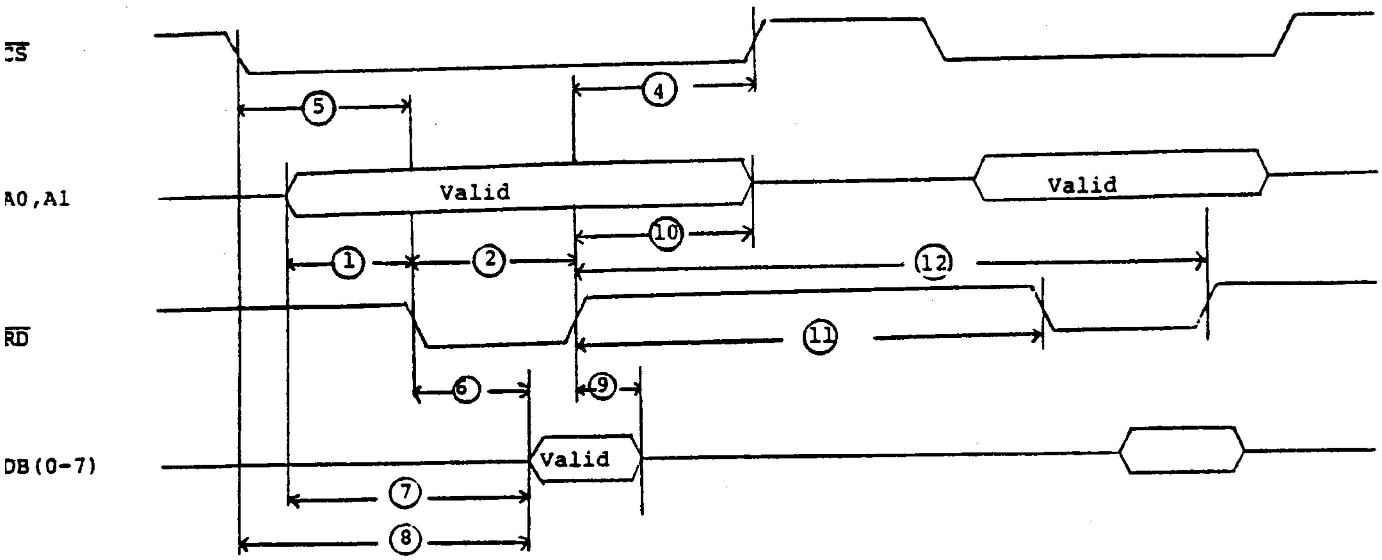
Number	Symbol	Parameter	Min	Max	Units	Comments
17	t_{chw}	$\overline{\text{CS}}$ Hold Time after $\overline{\text{WR}}$	Ø		nS	
18	t_{ahw}	Address Hold Time after $\overline{\text{WR}}$	Ø		nS	
19	t_{aw}	Address setup Time to $\overline{\text{WR}}$		50	nS	
20	t_{cw}	$\overline{\text{CS}}$ Setup Time to $\overline{\text{WR}}$	Ø		nS	
21	t_{dw}	Data Setup Time to $\overline{\text{WR}}$		50	nS	
22	t_{ww}	$\overline{\text{WR}}$ Pulse Width	200		nS	
23	t_{wd}	Data Hold Time to $\overline{\text{WR}}$	Ø		nS	
24	t_{wdead1}	Write Dead Time (Address)	100		nS	
25	t_{cycw}	Write Cycle Time (Address)	300		nS	
26	t_{alewr}	ALE to $\overline{\text{WR}}$	50		nS	
27	$t_{cycwale}$	Write Cycle Time (ALE)	400		nS	
28	t_{wdead2}	Write Dead Time (ALE)	200		nS	
29	t_{dwa}	Data Valid to ALE falling edge		50	nS	
30	t_{wda}	Data hold after ALE falling edge	Ø		nS	
31	t_{alerd}	ALE Falling edge to $\overline{\text{RD}}$ Falling edge	20		nS	



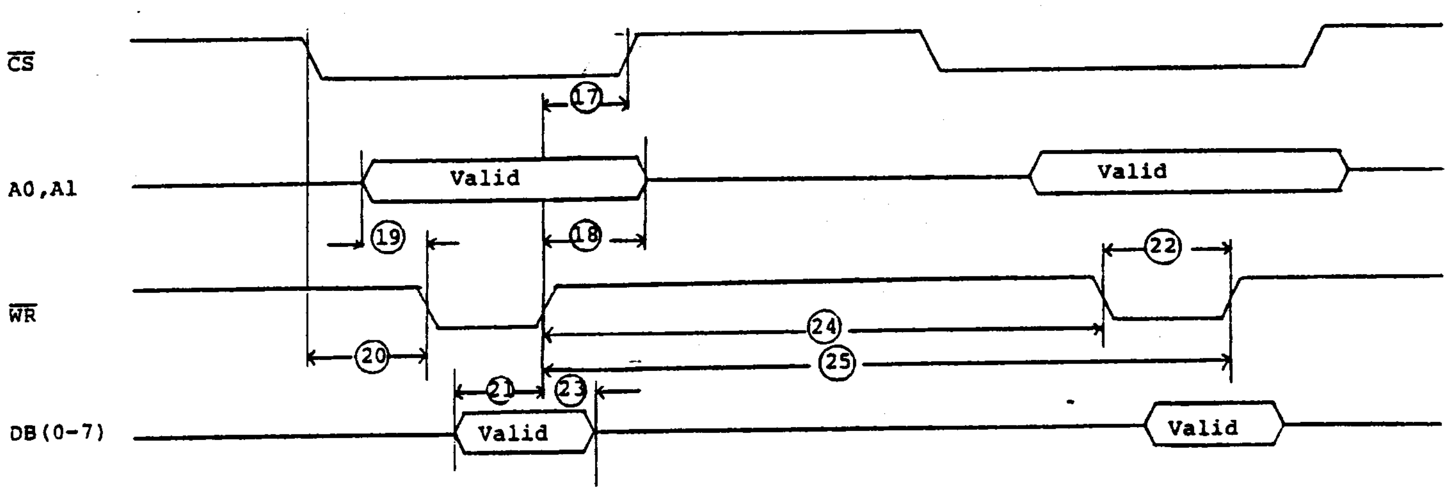
ALE Mode (AØ and A1 grounded, ALE bit in SOR = "1")
Read AMY Cycle



ALE Mode (AØ and A1 grounded, ALE bit in SOR = "1")
Write AMY Cycle



Address Pin Mode (ALE pin grounded, ALE bit in SOR = "Ø")
Read AMY Cycle



Address Pin Mode (ALE pin grounded, ALE bit in SOR = "Ø")
Write AMY Cycle

APPENDIX I.

Table A shows the 13 bit tone values which correspond to full semitone steps on a piano keyboard. For example, Note A (440 Hz) will be reached if a fundamental frequency envelope reaches a destination value of 5004 Decimal (138C Hex). At a 4 MHz internal clock rate the actual frequency will be 440.04 Hz. The MSB and LSB fields show the Decimal values of the Destination MSB and LSB fields corresponding to the Atari Tone value.

Table B is in the same format as Table A, but the "Note" field was dropped as the values listed are "in between" 2 semitones (or notes on a piano). Table B shows that the actual frequency resolution at 440 Hz is approximately 0.4 Hz (1.5 cents).

Table C shows actual semitone/sec and decibel/sec slopes achieved by various 8 bit slope values. The M (mantissa) and E (exponent) fields are separated to give a feeling for the exponential coding scheme of slope byte. (Data valid for 4 MHz internal clock frequency and 64 harmonic mode).

TABLE A

Atari Tone (DEC)	MSB (HEX)	LSB (HEX)	FREQ (HZ)	NOTE
140	0	8C	5.4	F
204	0	CC	5.7	F#/Gb
268	1	C	6.1	G
332	1	4C	6.4	G#/Ab
396	1	8C	6.8	A
460	1	CC	7.2	A#/Bb
524	2	C	7.7	B
588	2	4C	8.1	C
652	2	8C	8.6	C#/Db
716	2	CC	9.1	D
780	3	C	9.7	D#/Eb
844	3	4C	10.3	E
908	3	8C	10.9	F
972	3	CC	11.5	F#/Gb
1036	4	C	12.2	G
1100	4	4C	12.9	G#/Ab
1164	4	8C	13.7	A
1228	4	CC	14.5	A#/Bb
1292	5	C	15.4	B
1356	5	4C	16.3	C
1420	5	8C	17.3	C#/Db
1484	5	CC	18.3	D
1548	6	C	19.4	D#/Eb
1612	6	4C	20.6	E
1676	6	8C	21.8	F
1740	6	CC	23.1	F#/Gb
1804	7	C	24.5	G
1868	7	4C	25.9	G#/Ab
1932	7	8C	27.5	A
1996	7	CC	29.1	A#/Bb
2060	8	C	30.8	B
2124	8	4C	32.7	C
2188	8	8C	34.6	C#/Db
2252	8	CC	36.7	D
2316	9	C	38.8	D#/Eb
2380	9	4C	41.2	E
2444	9	8C	43.6	F
2508	9	CC	46.2	F#/Gb
2572	A	C	49	G
2636	A	4C	51.9	G#/Ab
2700	A	8C	55	A
2764	A	CC	58.2	A#/Bb
2828	B	C	61.7	B
2892	B	4C	65.4	C
2956	B	8C	69.3	C#/Db
3020	B	CC	73.4	D
3084	C	C	77.7	D#/Eb

TABLE A (continued)

Atari Tone (DEC)	MSB (HEX)	LSB (HEX)	FREQ (HZ)	NOTE
3148	C	4C	82.4	E
3212	C	8C	87.3	F
3276	C	CC	92.5	F#/Gb
3340	D	C	98	G
3404	D	4C	103.8	G#/Ab
3468	D	8C	110	A
3532	D	CC	116.5	A#/Bb
3596	E	C	123.4	B
3660	E	4C	130.8	C
3724	E	8C	138.6	C#/Db
3788	E	CC	146.8	D
3852	F	C	155.5	D#/Eb
3916	F	4C	164.8	E
3980	F	8C	174.6	F
4044	F	CC	185	F#/Gb
4108	10	C	196	G
4172	10	4C	207.6	G#/Ab
4236	10	8C	220	A
4300	10	CC	233.1	A#/Bb
4364	11	C	246.9	B
4428	11	4C	261.6	C
4492	11	8C	277.2	C#/Db
4556	11	CC	293.6	D
4620	12	C	311.1	D#/Eb
4684	12	4C	329.6	E
4748	12	8C	349.2	F
4812	12	CC	370	F#/Gb
4876	13	C	392	G
4940	13	4C	415.3	G#/Ab
5004	13	8C	440	A
5068	13	CC	466.2	A#/Bb
5132	14	C	493.9	B
5196	14	4C	523.3	C
5260	14	8C	554.4	C#/Db
5324	14	CC	587.3	D
5388	15	C	622.3	D#/Eb
5452	15	4C	659.3	E
5516	15	8C	698.5	F
5580	15	CC	740	F#/Gb
5644	16	C	784	G
5708	16	4C	830.7	G#/Ab
5772	16	8C	880	A
5836	16	CC	932.4	A#/Bb
5900	17	C	987.8	B
5964	17	4C	1046.6	C
6028	17	8C	1108.8	C#/Db

TABLE A (continued)

Atari Tone (DEC)	MSB (HEX)	LSB (HEX)	FREQ (HZ)	NOTE
6092	17	CC	1174.7	D
6156	18	C	1244.6	D#/Eb
6220	18	4C	1318.6	E
6284	18	8C	1397	F
6348	18	CC	1480.1	F#/Gb
6412	19	C	1568.1	G
6476	19	4C	1661.4	G#/Ab
6540	19	8C	1760.1	A
6604	19	CC	1864.8	A#/Bb
6668	1A	C	1975.7	B
6732	1A	4C	2093.2	C
6796	1A	8C	2217.7	C#/Db
6860	1A	CC	2349.5	D
6924	1B	C	2489.2	D#/Eb
6988	1B	4C	2637.3	E
7052	1B	8C	2794.1	F
7116	1B	CC	2960.2	F#/Gb
7180	1C	C	3136.3	G
7244	1C	4C	3322.7	G#/Ab
7308	1C	8C	3520.3	A
7372	1C	CC	3729.7	A#/Bb
7436	1D	C	3951.4	B
7500	1D	4C	4186.4	C
7564	1D	8C	4435.4	C#/Db
7628	1D	CC	4699.1	D
7692	1E	C	4978.5	D#/Eb
7756	1E	4C	5274.6	E
7820	1E	8C	5588.2	F
7884	1E	CC	5920.5	F#/Gb
7948	1F	C	6272.6	G
8012	1F	4C	6645.5	G#/Ab
8076	1F	8C	7040.7	A
8140	1F	CC	7459.4	A#/Bb

TABLE B

Atari Tone (DEC)	MSB (HEX)	LSB (HEX)	FREQ (HZ)
4941	13	4D	415.7
4942	13	4E	416
4943	13	4F	416.4
4944	13	50	416.8
4945	13	51	417.2
4946	13	52	417.5
4947	13	53	417.9
4948	13	54	418.3
4949	13	55	418.7
4950	13	56	419.1
4951	13	57	419.4
4952	13	58	419.8
4953	13	59	420.2
4954	13	5A	420.6
4955	13	5B	421
4956	13	5C	421.3
4957	13	5D	421.7
4958	13	5E	422.1
4959	13	5F	422.5
4960	13	60	422.9
4961	13	61	423.2
4962	13	62	423.6
4963	13	63	424
4964	13	64	424.4
4965	13	65	424.8
4966	13	66	425.2
4967	13	67	425.5
4968	13	68	425.9
4969	13	69	426.3
4970	13	6A	426.7
4971	13	6B	427.1
4972	13	6C	427.5
4973	13	6D	427.8
4974	13	6E	428.2
4975	13	6F	428.6
4976	13	70	429
4977	13	71	429.4
4978	13	72	429.8
4979	13	73	430.2
4980	13	74	430.6
4981	13	75	431
4982	13	76	431.3
4983	13	77	431.7
4984	13	78	432.1
4985	13	79	432.5
4986	13	7A	432.9
4987	13	7B	433.3

Range: 2 semitones
Resolution: 1 Atari Tone (1/64 st)
Centered around A (440 Hz)

TABLE B (continued)

Atari Tone (DEC)	MSB (HEX)	LSB (HEX)	FREQ (HZ)
4988	13	7C	433.7
4989	13	7D	434.1
4990	13	7E	434.5
4991	13	7F	434.9
4992	13	80	435.3
4993	13	81	435.6
4994	13	82	436
4995	13	83	436.4
4996	13	84	436.8
4997	13	85	437.2
4998	13	86	437.6
4999	13	87	438
5000	13	88	438.4
5001	13	89	438.8
5002	13	8A	439.2
5003	13	8B	439.6
5004	13	8C	440
5005	13	8D	440.4
5006	13	8E	440.8
5007	13	8F	441.2
5008	13	90	441.6
5009	13	91	442
5010	13	92	442.4
5011	13	93	442.8
5012	13	94	443.2
5013	13	95	443.6
5014	13	96	444
5015	13	97	444.4
5016	13	98	444.8
5017	13	99	445.2
5018	13	9A	445.6
5019	13	9B	446
5020	13	9C	446.4
5021	13	9D	446.8
5022	13	9E	447.2
5023	13	9F	447.6
5024	13	A0	448
5025	13	A1	448.4
5026	13	A2	448.8
5027	13	A3	449.2
5028	13	A4	449.6
5029	13	A5	450
5030	13	A6	450.4
5031	13	A7	450.8
5032	13	A8	451.3
5033	13	A9	451.7
5034	13	AA	452.1

TABLE B (continued)

Atari Tone (DEC)	MSB (HEX)	LSB (HEX)	FREQ (HZ)
5035	13	AB	452.5
5036	13	AC	452.9
5037	13	AD	453.3
5038	13	AE	453.7
5039	13	AF	454.1
5040	13	B0	454.5
5041	13	B1	454.9
5042	13	B2	455.3
5043	13	B3	455.8
5044	13	B4	456.2
5045	13	B5	456.6
5046	13	B6	457
5047	13	B7	457.4
5048	13	B8	457.8
5049	13	B9	458.2
5050	13	BA	458.6
5051	13	BB	459.1
5052	13	BC	459.5
5053	13	BD	459.9
5054	13	BE	460.3
5055	13	BF	460.7
5056	13	C0	461.1
5057	13	C1	461.6
5058	13	C2	462
5059	13	C3	462.4
5060	13	C4	462.8
5061	13	C5	463.2
5062	13	C6	463.6
5063	13	C7	464.1
5064	13	C8	464.5
5065	13	C9	464.9
5066	13	CA	465.3
5067	13	CB	465.7

TABLE C

+ SLOPE (HEX)	- SLOPE (HEX)	SEMI/SEC	DB/SEC	M (HEX)	E (HEX)
0	80	0	0	0	0
1	9F	0.11	1.9	1	0
2	9E	0.23	3.81	2	0
3	9D	0.35	5.72	3	0
4	9C	0.47	7.62	4	0
5	9B	0.59	9.53	5	0
6	9A	0.71	11.44	6	0
7	99	0.83	13.35	7	0
8	98	0.95	15.25	8	0
9	97	1.07	17.16	9	0
A	96	1.19	19.07	A	0
B	95	1.31	20.98	B	0
C	94	1.43	22.88	C	0
D	93	1.54	24.79	D	0
E	92	1.66	26.7	E	0
F	91	1.78	28.61	F	0
10	90	1.9	30.51	10	0
11	8F	2.02	32.42	11	0
12	8E	2.14	34.33	12	0
13	8D	2.26	36.23	13	0
14	8C	2.38	38.14	14	0
15	8B	2.5	40.05	15	0
16	8A	2.62	41.96	16	0
17	89	2.74	43.86	17	0
18	88	2.86	45.77	18	0
19	87	2.98	47.68	19	0
1A	86	3.09	49.59	1A	0
1B	85	3.21	51.49	1B	0
1C	84	3.33	53.4	1C	0
1D	83	3.45	55.31	1D	0
1E	82	3.57	57.22	1E	0
1F	81	3.69	59.12	1F	0
20	A0	0	0	0	1
21	BF	0.47	7.62	1	1
22	BE	0.95	15.25	2	1
23	BD	1.43	22.88	3	1
24	BC	1.9	30.51	4	1
25	BB	2.38	38.14	5	1
26	BA	2.86	45.77	6	1
27	B9	3.33	53.4	7	1
28	B8	3.81	61.03	8	1
29	B7	4.29	68.66	9	1
2A	B6	4.76	76.29	A	1
2B	B5	5.24	83.92	B	1
2C	B4	5.72	91.55	C	1
2D	B3	6.19	99.18	D	1
2E	B2	6.67	106.81	E	1

TABLE C (continued)

+ SLOPE (HEX)	- SLOPE (HEX)	SEMI/SEC	DB/SEC	M (HEX)	E (HEX)
2F	B1	7.15	114.44	F	1
30	B0	7.62	122.07	10	1
31	AF	8.1	129.69	11	1
32	AE	8.58	137.32	12	1
33	AD	9.05	144.95	13	1
34	AC	9.53	152.58	14	1
35	AB	10.01	160.21	15	1
36	AA	10.49	167.84	16	1
37	A9	10.96	175.47	17	1
38	A8	11.44	183.1	18	1
39	A7	11.92	190.73	19	1
3A	A6	12.39	198.36	1A	1
3B	A5	12.87	205.99	1B	1
3C	A4	13.35	213.62	1C	1
3D	A3	13.82	221.25	1D	1
3E	A2	14.3	228.88	1E	1
3F	A1	14.78	236.51	1F	1
40	C0	0	0	0	2
41	DF	1.9	30.51	1	2
42	DE	3.81	61.03	2	2
43	DD	5.72	91.55	3	2
44	DC	7.62	122.07	4	2
45	DB	9.53	152.58	5	2
46	DA	11.44	183.1	6	2
47	D9	13.35	213.62	7	2
48	D8	15.25	244.14	8	2
49	D7	17.16	274.65	9	2
4A	D6	19.07	305.17	A	2
4B	D5	20.98	335.69	B	2
4C	D4	22.88	366.21	C	2
4D	D3	24.79	396.72	D	2
4E	D2	26.7	427.24	E	2
4F	D1	28.61	457.76	F	2
50	D0	30.51	488.28	10	2
51	CF	32.42	518.79	11	2
52	CE	34.33	549.31	12	2
53	CD	36.23	579.83	13	2
54	CC	38.14	610.35	14	2
55	CB	40.05	640.86	15	2
56	CA	41.96	671.38	16	2
57	C9	43.86	701.9	17	2
58	C8	45.77	732.42	18	2
59	C7	47.68	762.93	19	2
5A	C6	49.59	793.45	1A	2
5B	C5	51.49	823.97	1B	2
5C	C4	53.4	854.49	1C	2
5D	C3	55.31	885	1D	2

TABLE C (continued)

+ SLOPE (HEX)	- SLOPE (HEX)	SEMI/SEC	DB/SEC	M (HEX)	E (HEX)
5E	C2	57.22	915.52	1E	2
5F	C1	59.12	946.04	1F	2
60	E0	0	0	0	3
61	FF	7.62	122.07	1	3
62	FE	15.25	244.14	2	3
63	FD	22.88	366.21	3	3
64	FC	30.51	488.28	4	3
65	FB	38.14	610.35	5	3
66	FA	45.77	732.42	6	3
67	F9	53.4	854.49	7	3
68	F8	61.03	976.56	8	3
69	F7	68.66	1098.63	9	3
6A	F6	76.29	1220.7	A	3
6B	F5	83.92	1342.77	B	3
6C	F4	91.55	1464.84	C	3
6D	F3	99.18	1586.91	D	3
6E	F2	106.81	1708.98	E	3
6F	F1	114.44	1831.05	F	3
70	F0	122.07	1953.12	10	3
71	EF	129.69	2075.19	11	3
72	EE	137.32	2197.26	12	3
73	ED	144.95	2319.33	13	3
74	EC	152.58	2441.4	14	3
75	EB	160.21	2563.47	15	3
76	EA	167.84	2685.54	16	3
77	E9	175.47	2807.61	17	3
78	E8	183.1	2929.68	18	3
79	E7	190.73	3051.75	19	3
7A	E6	198.36	3173.82	1A	3
7B	E5	205.99	3295.89	1B	3
7C	E4	213.62	3417.96	1C	3
7D	E3	221.25	3540.03	1D	3
7E	E2	228.88	3662.1	1E	3
7F	E1	236.51	3784.17	1F	3

APPENDIX II

Musical Specifications

Given an internal CLK frequency of 4 MHz with 64 Harmonics enabled:

Amplitude Dynamic Range	63.75 dB
Minimum Amplitude Slope	1.91 dB/sec
Maximum Amplitude Slope	3784 dB/sec
Fundamental Frequency Range	~ 4.8 Hz to 7.8 KHz (10 2/3 octave range)
Minimum Fundamental Frequency Slope	5.97 cents*/sec
Maximum Fundamental Frequency Slope	118 semitones/sec = 9.85 octave range)
Maximum Amplitude Increment	31/128 = 0.242 dB
Fundamental Frequency Increment	1/64 semitones = 1.56 cents
Fundamental Frequency Resolution	1/64 semitones = 1.56 cents
Harmonic Amplitude Resolution	1/4 dB
Number of Harmonics	64 (maximum)
Number of Voices	8 (maximum)
Number of Harmonics/Voice	Any multiple of 2
Harmonic Distortion	$<$ 1%

* 1 cent = 1/100 of a semitone