

Engineering Hardware Specification
of the
Atari ST Computer System

The Atari Corporation
Sunnyvale, California

24 January 1985

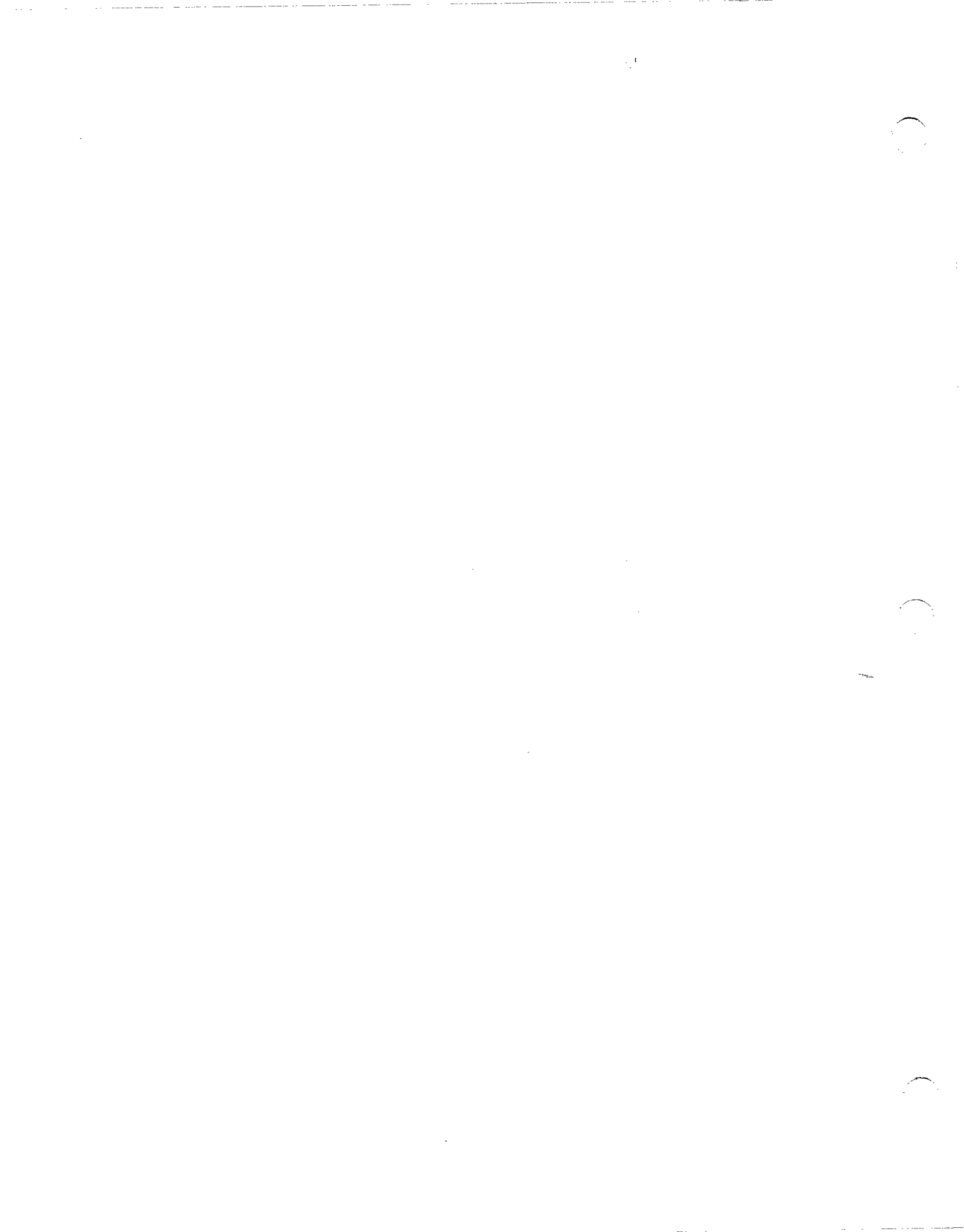
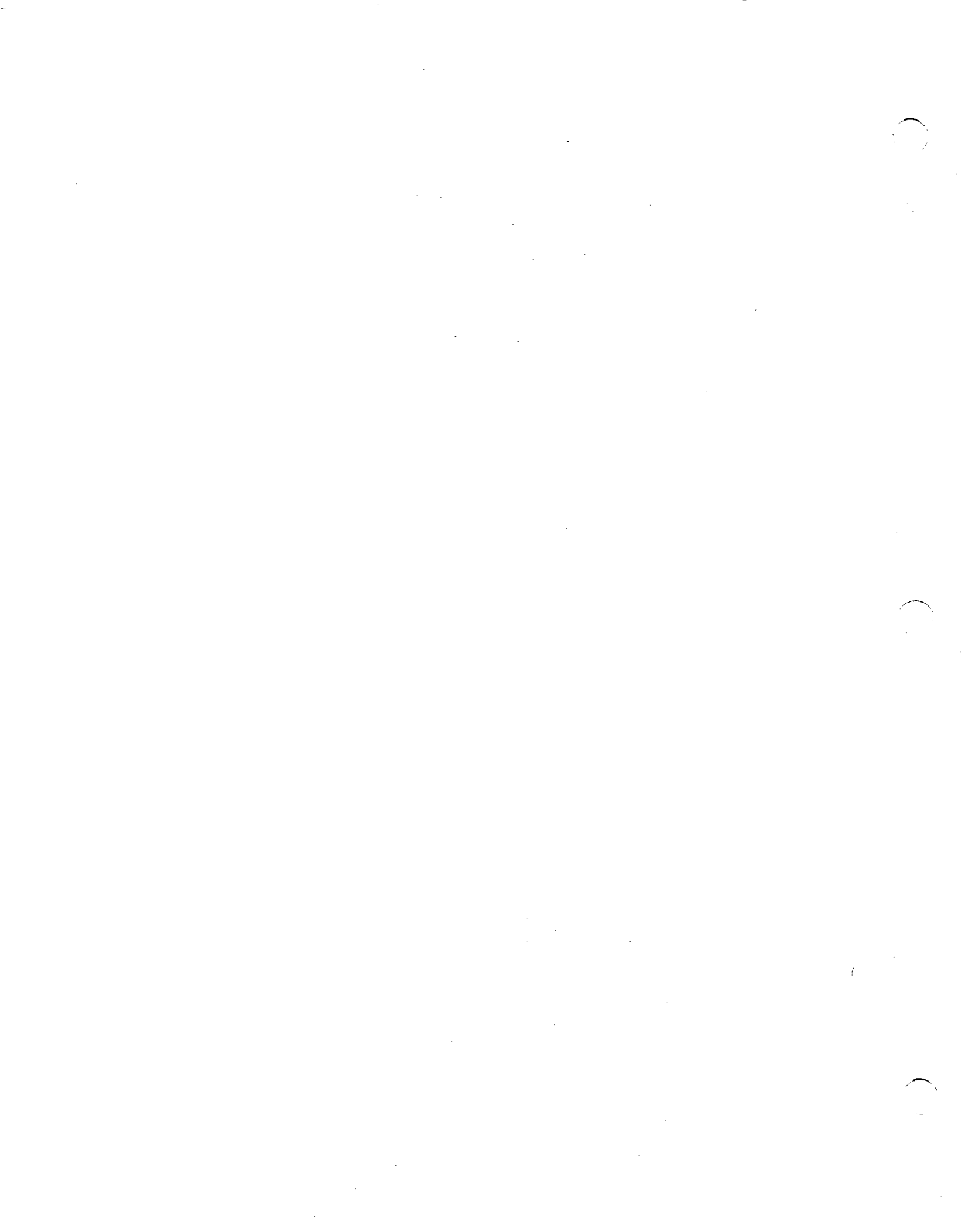


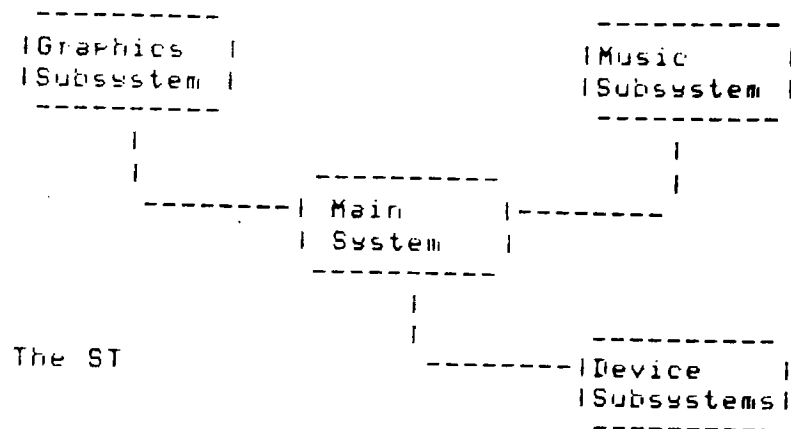
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1. System Architecture



The hardware architecture of the Atari Corporation ST computer system consists of a main system, a graphics subsystem, a music subsystem, and several device subsystems (most of the device subsystems require ST resident intelligence). The ST is based on the Motorola MC68000 16 bit data/24 bit address microprocessor unit capable of directly accessing up to 16 Mbytes of ROM and RAM memory. Hardware features of the ST computer system include:

Main System

- o 16 bit data/24 bit address 8 MHz microprocessor unit
- o 192 Kbyte ROM, cartridge expandable to 320 Kbyte
- o 128 or 512 Kbyte RAM
- o direct memory access support

Graphics Subsystem

- o 32 Kbyte BitMap video display memory (from above)
- o 320 x 200 pixel, 16 color palette from 512 selections
- o 640 x 200 pixel, 4 color palette from 512 selections
- o 640 x 400 pixel, monochrome

Music Subsystem

- o Programmable sound synthesizer
- o musical instrument network communication

Device Subsystems

- o intelligent keyboard
- o two button mouse
- o television receiver (factory set NTSC or PAL) interface
- o composite, RGB, and monochrome monitor interfaces
- o printer parallel interface

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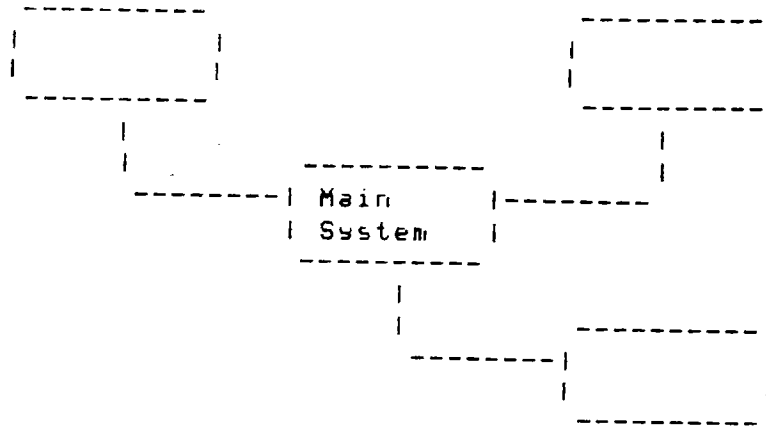
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- o RS232 serial interface
- o MIDI musical instrument interface
- o on board floppy disk controller and interface
- o hard disk drive interface

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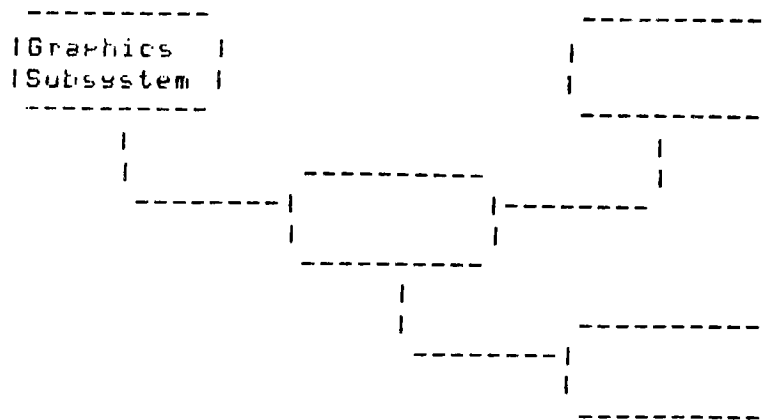
2. Main System



2.1. Microprocessor Unit

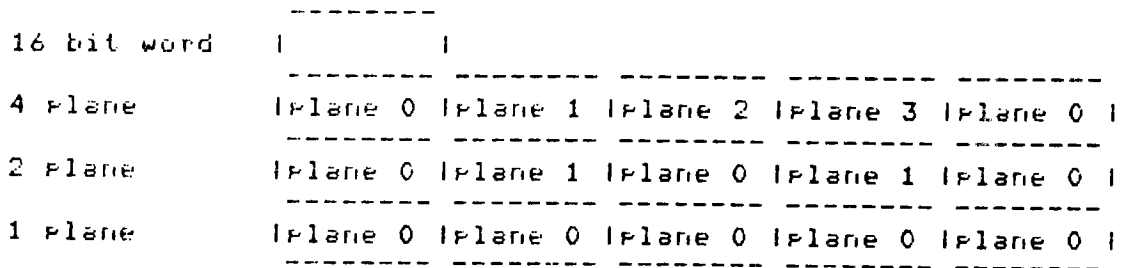
The ST computer system is based on an 8 MHz Motorola MC68000 16 bit data/24 bit address microprocessor unit (with an internal 32 bit architecture). Some features of the MC68000 are: eight 32 bit data registers, nine 32 bit address registers, a 16 Mbyte direct addressing range, 14 addressing modes, memory mapped I/O, five data types, and a 56 instruction set.

3. Graphics Subsystem



3.1. Video Display Memory

Video display memory is configured as n logical planes interwoven by 16 bit words into contiguous memory to form one 32 Kbyte Physical Plane starting at a 256 byte half page boundary. The following is a diagram of possible physical configurations of video display memory:



Display memory resides as part of main memory and has an identical bit, byte, and word arrangement with the physical screen origin located at top left:

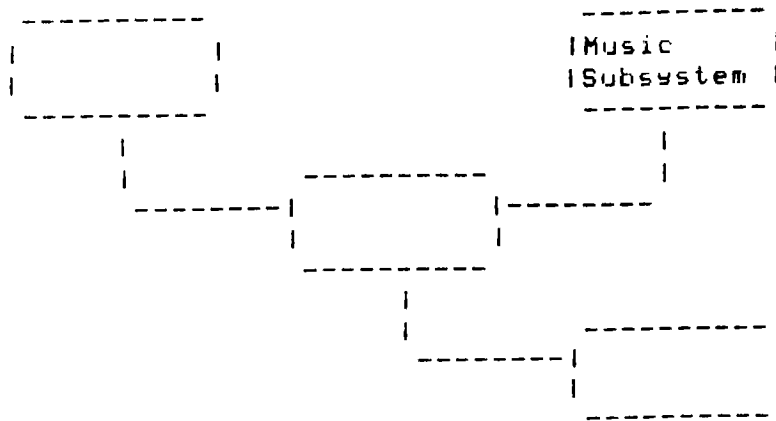
	high	low
word 0	byte 0	byte 1
	fedcba98	76543210

3.2. Video Configuration

The ST possesses three modes of video configuration: 320 x 200 resolution with 4 planes, 640 x 200 resolution with 2 planes, and 640 x 400 resolution with 1 plane. A sixteen word color lookup palette is provided with nine bits of color per entry. The sixteen color palette registers contain three bits of red, green, and blue aligned on low nibble boundaries. Eight levels of red, eight levels of green, and eight levels of blue produce a total of 512 possible colors.

In 320 x 200 4 plane mode all sixteen palette colors can be indexed, while in 640 x 200 2 plane mode only the first four palette entries are applicable. In 640 x 400 monochrome mode the color palette is bypassed altogether and is instead provided with an inverter for inverse video controlled by bit 0 of palette color 0 (color palette memory is arranged the same as main memory). Palette color 0 is also used to assign a border color in multi-plane mode and a white or black border in monochrome mode depending on bit 0 (white 1, black 0).

4. Music Subsystem



4.1. Sound Synthesizer

The Atari ST Programmable Sound Generator produces music synthesis, sound effects, and audio feedback (e.g. alarms and key clicks). With an applied clock input of 2 MHz, the PSG is capable of providing a frequency response range between 30 Hz (audible) and 125 KHz (post-audible). The generator places a minimal amount of processing burden on the main system (which acts as the sequencer) and has the ability to perform using three independent voice channels. The three sound channel outputs are mixed and sent to a television receiver or monitor speaker (the PSG has built in digital to analog converters).

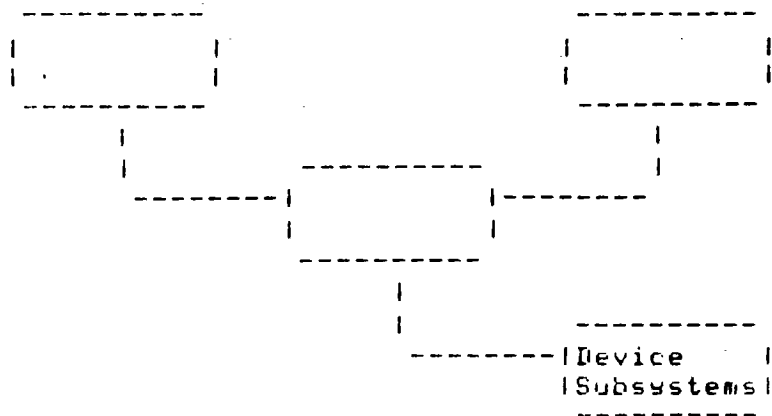
The PSG's tone generator registers control a basic square wave while the noise generator register controls a frequency modulated square wave of pseudo random pulse width. Tones and noise can be mixed over individual channels by using the mixer control register. The amplitude registers allow the specification of a fixed amplitude or of a variable amplitude when used with the envelope generator. The envelope generator registers permit the entry of a skewed attack-decay-sustain-release envelope in the form of a continue-attack-alternate-hold envelope.

4.2. Musical Instrument Communication

The Sequential Circuits Incorporated Musical Instrument Digital Interface (MIDI) allows the integration of the ST with music synthesizers, sequencers, drum boxes, and other devices possessing MIDI interfaces. High speed (31.25 Kbaud) serial communication of keyboard and program information is provided by two ports, MIDI OUT and MIDI IN (MIDI OUT also supports the optional MIDI THRU port).

The MIDI bus permits up to 16 channels in one of three network addressing modes: Omni (all units addressed simultaneously, power up default), Poly (each unit addressed separately), and Mono (each unit voice addressed separately). Information is communicated via five types of data format (data bytes, most significant bit: status 1, data 0) which are prioritized from highest to lowest as: System Reset (default conditions, should not be sent on power up to avoid deadlock), System Exclusive (manufacturer unique data: Sequential Circuits, Kawai, Roland, Korg, Yamaha), System Real Time (synchronization), System Common (broadcast), and Channel (note selections, program data, etc).

5. Device Subsystems



5.1. RS232 Interface

The ST RS232 interface provides voltage level synchronous or asynchronous serial communication. Five EIA RS232C handshake control signals are supported: Request To Send and Data Terminal Ready are transmitted through the PSG I/O Port A while Clear To Send, Data Carrier Detect, and Ring Indicator are received through another component. The transmit and receive clock inputs can support asynchronous data transfer rates from 50 to 19200 baud.

6. Memory Map

The first 2 Kbyte of ST memory is reserved for the exception vector table and supervisor stack. This area along with I/O space is protected for supervisor references only. Accessing supervisor protected areas while in the user state will result in a bus error. A 4 word portion of ROM is shadowed at the start of RAM for the reset stack pointer and program counter. Writing to this area or any ROM location will also result in a bus error. The following is a map of ST memory:

00 0000	ROM		Reset: Supervisor Stack Pointer
00 0004	ROM		Reset: Program Counter
00 0008	RAM		0 Kbyte RAM

.			
02 0000	RAM		128 Kbyte RAM

.			
08 0000	RAM		512 Kbyte RAM

:			
:			
:			

fe 0000	ROM		
fe 0000	ROM		
fe 0004	ROM		
fe 0008	ROM		
fe ffff	ROM		

.			
:			
:			

ff 8000	I/O		
ff 8200	I/O		
ff 8400	I/O		
ff 8600	I/O		
ff 8800	I/O		

.			

ff fa00	I/O		
ff fc00	I/O		

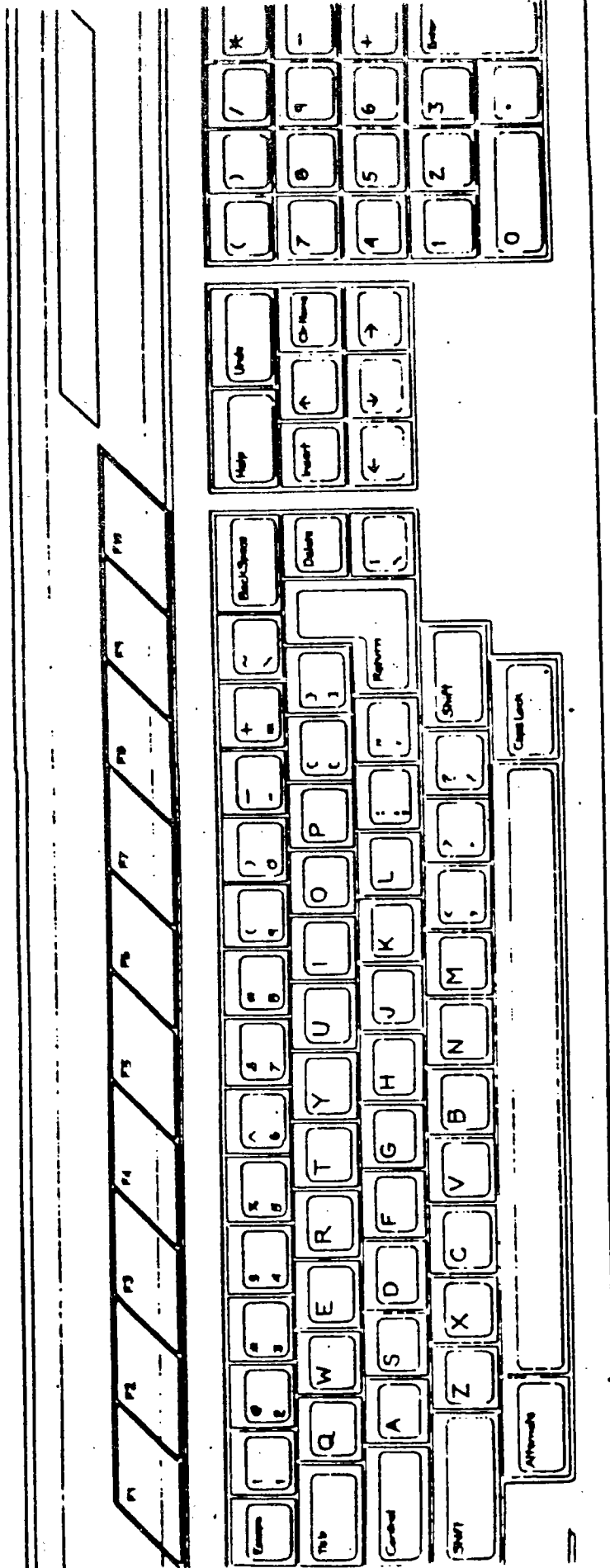
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Appendix A -- ST Keyboard Layout

The surface of the Atari Intelligent Keyboard is formed from four distinct ergonomic units: a QWERTY typewriter matrix, a function key array, a screen control cluster, and a calculator numeric keypad. As a whole, the keyboard layout is DEC VT100-like with the exception of the following items:

- o removed keys -- [break], [line feed], [no scroll], [set up],
- o repositioned keys -- [caps lock], cursor control keys, programmable function keys,
- o added keys -- [alternate], [help], [undo], [insert], [clear/home], 10 programmable function keys,
- o improvements -- DEC VT200-style inverted T cursor control keys, full calculator function numeric keypad.

Please note that the left [shift] key is intentionally large to allow space for an extra ISO required key.



THE KEYBOARD

