Atari Hardware Description V1.2

Done by Joerg Hohwiller/Beweise of DNS

Most information for this document are from ST intern, Hardware-Text by Dan Hollis and of course FalconDoku from Chis/Aura. But I wanted to have all information in one short& compact list. So this is not a full documentation.

If you find mistakes or have more information please update or write me. I hope you like it... (Key is below)

			Exeption Vectors	
$00000000.L	R-	XPT_SPR	SSP after Reset	
$00000004.L	R-	XPT_PCR	PC after Reset	
$00000008.L	RW	XPT_BUS	Bus Error	
$0000000C.L	RW	XPT_ADR	Address Error	
$00000010.L	RW	XPT_ILL	Illegal Instruction	
$00000014.L	RW	XPT_DBZ	Devide by Zero	
$00000018.L	RW	XPT_CHK	Chk, Chk2 Instruction	
$0000001C.L	RW	XPT_TRV	Trapv Instruction	
$00000020.L	RW	XPT_PRV	Privilege Violation	
$00000024.L	RW	XPT_TRC	Trace	
$00000028.L	RW	XPT_LNA	Linea	
$0000002C.L	RW	XPT_LNF	Linef	
$00000030.L	RW	-	reserved	
$00000034.L	RW	XPT_FPU	Coprocessor Protocol Violation	030+
$00000038.L	RW	XPT_FRM	Format Error	010+
$0000003C.L	RW	XPT_DSP	DSP Transfer Interrupt	*
$00000040.L	RW	-	reserved	
$00000044.L	RW	-	reserved	
$00000048.L	RW	-	reserved	
$0000004C.L	RW	-	reserved	
$00000050.L	RW	-	reserved	
$00000054.L	RW	-	reserved	
$00000058.L	RW	-	reserved	
$0000005C.L	RW	-	reserved	
$00000060.L	RW	XPT_SPU	Spurious Interrupt	
$00000064.L	RW	XPT_LV1	Level 1 -	
$00000068.L	RW	XPT_HBL	Level 2 - HBL	
$0000006C.L	RW	XPT_LV3	Level 3 -	
$00000070.L	RW	XPT_VBL	Level 4 - VBL	
$00000074.L	RW	XPT_LV5	Level 5 - SCC	
$00000078.L	RW	XPT_LV6	Level 6 - MFP	
$0000007C.L	RW	XPT_LV7	Level 7 -	
$00000080.L	RW	XPT_T00	Trap #00	
$00000084.L	RW	XPT_T01	Trap #01	
$00000088.L	RW	XPT_T02	Trap #02	
$0000008C.L	RW	XPT_T03	Trap #03	
$00000090.L	RW	XPT_T04	Trap #04	
$00000094.L	RW	XPT_T05	Trap #05	
$00000098.L	RW	XPT_T06	Trap #06	
$0000009C.L	RW	XPT_T07	Trap #07	
$000000A0.L	RW	XPT_T08	Trap #08	
$000000A4.L	RW	XPT_T09	Trap #09	
$000000A8.L	RW	XPT_T10	Trap #10	
$000000AC.L	RW	XPT_T11	Trap #11	
$000000B0.L	RW	XPT_T12	Trap #12	
$000000B4.L	RW	XPT_T13	Trap #13	
$000000B8.L	RW	XPT_T14	Trap #14	
$000000BC.L	RW	XPT_T15	Trap #15	
$000000C0.L	RW	FPU_BOS	FFCP Branc or Set	020+
$000000C4.L	RW	FPU_INX	FFCP Inexact Result	020+
$000000C8.L	RW	FPU_DBZ	FFCP Devide by Zero	020+
$000000CC.L	RW	FPU_UNR	FFCP Underflow	020+
$000000D0.L	RW	FPU_OPE	FFCP Operand Error	020+
$000000D4.L	RW	FPU_OVR	FFCP Overflow	020+
$000000D8.L	RW	FPU_NAN	FFCP signaling NAN	020+
$000000DC.L	RW	-	reserved	

```
$000000E0.L|RW|XPT_MMU|MMU Configuration Error                          |030+
$000000E4.L|RW|   -   |reserved                                         |
$000000E8.L|RW|   -   |reserved                                         |
$000000EC.L|RW|   -   |reserved                                         |
$000000F0.L|RW|   -   |reserved                                         |
$000000F4.L|RW|   -   |reserved                                         |
$000000F8.L|RW|   -   |reserved                                         |
$000000FC.L|RW|   -   |reserved                                         |
$00000100.L|RW|XPT_CTR|B0 Centronix busy                                 |*
$00000104.L|RW|XPT_DCD|B1 RS232 DCD                                      |*
$00000108.L|RW|XPT_CTS|B2 RS232 CTS                                      |*
$0000010C.L|RW|XPT_BLT|B3 Blitter Done                                  |*BLT
$00000110.L|RW|XPT_T_D|B4 Timer D                                       |*
$00000114.L|RW|XPT_T_C|B5 Timer C                                       |*
$00000118.L|RW|XPT_KBD|B6 IKBD/MIDI                                     |*
$0000011C.L|RW|XPT_FDC|B7 FDC/HDC                                       |*
$00000120.L|RW|XPT_T_B|A0 Timer B                                       |*
$00000124.L|RW|XPT_XMT|A1 Transmit Error                                |*
$00000128.L|RW|XPT_EMP|A2 Transmit Buffer empty                         |*
$0000012C.L|RW|XPT_REC|A3 Receive Error                                 |*
$00000130.L|RW|XPT_FUL|A4 Receive Buffer full                          |*
$00000134.L|RW|XPT_T_A|A5 Timer A                                       |*
$00000138.L|RW|XPT_RNG|A6 RS232 Ring Indicator                         |*
$0000013C.L|RW|XPT_SND|A7 Monochrome Detect/Audio Subsystem            |*
$00000140.L|RW|   -   |User defined Vectors                             |
...........|RW|   -   |.....................                            |
$000003FC.L|RW|   -   |User defined Vectors                             |
===========#==#=======#=================================================#=====
----------------------|Random Access Memory                             |-----
===========#==#=======#=================================================#=====
$00000008.B|RW|RAM_TOP|RAM TOP                                          |
...........|RW|   -   |.......                                          |
$00CFFFFF.B|RW|RAM_END|RAM END (14MB)                                   |
===========#==#=======#=================================================#=====
----------------------|1BM System Read Only Memory                      |-----
===========#==#=======#=================================================#=====
$00E00000.B|R-|ROM_TOP|1MB ROM TOP                                      |F
...........|R-|   -   |...........                                      |F
$00F0003F.B|R-|ROM_END|1MB ROM END                                      |F
===========#==#=======#=================================================#=====
$00F00040.B|--|   -   |Illegal Address Space                            |
...........|--|   -   |.....................                            |
$00F9FFFF.B|--|   -   |Illegal Address Space                            |
===========#==#=======#=================================================#=====
----------------------|128KB Expanstion Cartidge Port                   |-----
===========#==#=======#=================================================#=====
$00FA0000.L|R-|ROM_PRT|Cartridge Magic($FA52235F=Diag,$ABCDEF42=User*)|
$00FA0004.L|R-|ROM_CAL|Call Diagnostic Cardridge                       |
...........|R-|   -   |............                                     |
$00FBFFFF.B|R-|   -   |ROM Port END                                     |
===========#==#=======#=================================================#=====
----------------------|192KB System Read Only Memory                   |-----
===========#==#=======#=================================================#=====
$00FC0000.B|--|   -   |192KB ROM TOP                                    |ST
...........|--|   -   |.............                                    |ST
$00FEFFFF.B|--|   -   |192KB ROM END                                    |ST
===========#==#=======#=================================================#=====
----------------------|IDE Bus                                          |-----
===========#==#=======#=================================================#=====
$FFFF0000. |  |       |                                                 |
$FFFF0009.B|  |IDE_NSC|Number of Sectors                                |
```

```
$FFFF000D.B|  |IDE_SCC|Sector count                                          |
$FFFF0011.B|  |IDE_CYL|Cylinder low                                          |
$FFFF0015.B|  |IDE_CYH|Cylinder high                                         |
$FFFF0019.B|  |IDE_H_D|Head/Drive Register                                   |
$FFFF001D.B|  |IDE_S_C|Read:Status Register/Write:Command Register           |
$FFFF0039.B|  |       |                                                      |
==========#==#=======#======================================================#=====
----------------------|Memory Controller,System Control                      |-----
==========#==#=======#======================================================#=====
$FFFF8001.B|RW|MEM_CTL|Memory Controller                                     |
$FFFF8006.W|RW|SYS_CTL|System Control              %MM______ _RS_bB_C  |F
           |  |       | Monitor Type (M0,M1)--------++       || || | |F
           |  |       | Monochrome Monitor----------00       || || | |F
           |  |       | RGB Monitor-----------------01       || || | |F
           |  |       | VGA Monitor-----------------10       || || | |F
           |  |       | TV--------------------------11       || || | |F
           |  |       | Reset 0:ignore resetvector------------+| || | |F
           |  |       | STE-compatible-I/O 0:off,1:on----------+ || | |F
           |  |       | Blitterflag 0:on,1:off-------------------+| | |F
           |  |       | Blitterspeed 0:half clock,1:full clock----+ | |F
           |  |       | CPUspeed 0:half clock,1:full clock----------+ |F
==========#==#=======#======================================================#=====
----------------------|DMA,VIDEL Controler                                   |-----
==========#==#=======#======================================================#=====
$FFFF8201.B|RW|VDL_VBH|Video Base Hi                                         |
$FFFF8203.B|RW|VDL_VBM|Video Base Mi                                         |
$FFFF8205.B|Rw|VDL_VCH|Video Count Hi                                        |
$FFFF8207.B|Rw|VDL_VCM|Video Count Mi                                        |
$FFFF8209.B|Rw|VDL_VCL|Video Count Lo                        %xxxxxxx_ |
$FFFF820A.B|RW|VDL_SYM|Sync mode                             %______VS |
           |  |       | Vfrequency 0:60hz(NTSC),1:50Hz(PAL)--------+| |
           |  |       | Sync 0:internal,1:external------------------+ |
$FFFF820D.B|RW|VDL_VBL|Video Base Lo                        %xxxxxxx_ |STE,F
$FFFF820E.B|RW|VDL_LOF|Line Offset                                       |STE,F
$FFFF820F.B|RW|   -   |Line Wide-1                                       |STE
$FFFF8210.W|RW|VDL_LWD|Line Wide in Words          %______xx xxxxxxxx |F
$FFFF8240.W|RW|VDL_STC|ST Pallete Register 00      %____rRRR gGGGbBBB |
...........|RW|   -   |.....................                             |
$FFFF825E.W|RW|   -   |ST Pallete Register 15                            |
$FFFF8260.B|RW|VDL_SSM|ST-Shift-Mode/TT-Shift-Mode          %_____xxx |
           |  |       | 320*200*4-------------------------------000 |
           |  |       | 640*200*2-------------------------------001 |
           |  |       | 640*400*1-------------------------------010 |
           |  |       | nute------------------------------------011 |
           |  |       | 640*480*4-------------------------------100 |TT
           |  |       | 1280*960*1------------------------------101 |TT
           |  |       | 320*480*8-------------------------------110 |TT
           |  |       | nute------------------------------------111 |TT
$FFFF8264.B|RW|VDL_HSH|H-Scroll Hi                              %____xxxx |F
$FFFF8265.B|RW|VDL_HSL|H-Scroll Lo - clears Line Wide          %____xxxx |STE,F
$FFFF8266.W|RW|VDL_FSM|Falcon Shift Mode           %_____2OT _HV8PPPP |F
           |  |       | 2 Color mode 0:off,1:on----------+||  ||||||| |F
           |  |       | Overlay mode 0:off,1:on----------+|  ||||||| |F
           |  |       | True(high) color 0:off,1:on--------+  ||||||| |F
           |  |       | Hsync 0:internal,1:external-----------+|||||| |F
           |  |       | Vsync 0:internal,1:external------------+||||| |F
           |  |       | 8 Bitplanes 0:off,1:on------------------+|||| |F
           |  |       | falcon Palette 16 of 256 colors----------++++ |F
$FFFF8280.W|RW|VDL_HHC|Horizontal Hold Counter     %_______x xxxxxxxx |F
$FFFF8282.W|RW|VDL_HHT|Horizontal Hold Timer       %_______x xxxxxxxx |F
$FFFF8284.W|RW|VDL_HBB|Horizontal Border Begin     %_______x xxxxxxxx |F
```

```
$FFFF8286.W|RW|VDL_HBE|Horizontal Border End       %_______x xxxxxxxx |F
$FFFF8288.W|RW|VDL_HDB|Horizontal Display Begin    %______Hx xxxxxxxx |F
           |  |        | 0:1.Halftline, 1:2.Halfline-------+          |F
$FFFF828A.W|RW|VDL_HDE|Horizontal Display End      %_______x xxxxxxxx |F
$FFFF828C.W|RW|VDL_HSS|Horizontal Sync Start       %_______x xxxxxxxx |F
$FFFF828E.W|RW|VDL_HFS|Horizontal FS               %_______x xxxxxxxx |F
$FFFF8290.W|RW|VDL_HEE|Horizontal EE               %_______x xxxxxxxx |F
$FFFF82A0.W|RW|VDL_VFC|Vertical Frequenz Counter   %_____xxx xxxxxxxx |F
$FFFF82A2.W|RW|VDL_VFT|Vertical Frequenz Timer     %_____xxx xxxxxxxx |F
$FFFF82A4.W|RW|VDL_VBB|Vertical Border Begin       %_____xxx xxxxxxxx |F
$FFFF82A6.W|RW|VDL_VBE|Vertical Border End         %_____xxx xxxxxxxx |F
$FFFF82A8.W|RW|VDL_VDB|Vertical Display Begin      %_____xxx xxxxxxxx |F
$FFFF82AA.W|RW|VDL_VDE|Vertical Display End        %_____xxx xxxxxxxx |F
$FFFF82AC.W|RW|VDL_VSS|Vertical Sync Start         %_____xxx xxxxxxxx |F
$FFFF82C0.W|RW|VDL_VCT|Video Control               %_______O BHVUSCMM |F
           |  |        | h-base-Offset 0:128cyc,1:64cyc-----+ |||||||| |F
           |  |        | Buswide 0:16bit,1:32bit--------------+|||||||| |F
           |  |        | Hsync 0:negative,1:positive-----------+|||||| |F
           |  |        | Vsync 0:negative,1:positive------------+||||| |F
           |  |        | Use FS & EE 0:on,1:off------------------+|||| |F
           |  |        | 15 halflinehSyncs at VBB-----------------+||| |F
           |  |        | video Clock 0:32Mhz,1:25.175Mhz-----------+|| |F
           |  |        | Monitor 0:Mono,1:RGB,2:VGA,3:TV------------++ |F
$FFFF82C2.W|RW|VDL_VMD|Video Mode                 %________ ____xxID |F
           |  |        | Pixclock:4,Divider:4(VGA)/16(STE)/4------00|| |F
           |  |        | Pixclock:2,Divider:2(VGA)/16(STE)/2------01|| |F
           |  |        | Pixclock:1,Divider:2(VGA)/16(STE)/1------10|| |F
           |  |        | nute-------------------------------------11|| |F
           |  |        | Interlace 0:off,1:on----------------------+| |F
           |  |        | Double Scan 0:off,1:on---------------------+ |F
==========#==#=======#=================================================#=====
----------------------|TT Palette Registers                            |-----
==========#==#=======#=================================================#=====
$FFFF8400.W|RW|TT__PAL|TT Palette Register 000                         |TT
...........|RW|   -   |.......................                         |TT
$FFFF85FE.W|RW|   -   |TT Palette Register 255                         |TT
==========#==#=======#=================================================#=====
----------------------|DMA,WD1772 Disk Controller                      |-----
==========#==#=======#=================================================#=====
$FFFF8604.W|RW|WDC_SEC|FDC/HDC Access/Sector Count                     |
$FFFF8606.W|R-|WDC_DMA|DMA Status                %_________ _____DSE |
           |  |        | Data request condition--------------------+|| |
           |  |        | Sector count 0:zero,1:not zero-------------+| |
           |  |        | DMA 0:no error,1:error----------------------+ |
           |-W|        |DMA Mode                   %_______W FD_SHAA_ |
           |  |        | 0:read,1:write----------------------+ || ||||  |
           |  |        | 0:HDC,1:FDC access-------------------+| ||||  |
           |  |        | DMA 0:on,1:off------------------------+ ||||  |
           |  |        | 0:FDC/HDC register 1:sector count-------+|||  |
           |  |        | 0:FDC,1:HDC access-----------------------+||  |
           |  |        | A1/A0 pin 0:low,1:high--------------------++  |
$FFFF8609.B|RW|WDC_BSH|DMA Base and Counter Hi                         |
$FFFF860B.B|RW|WDC_BSM|DMA Base and Counter Mi                         |
$FFFF860D.B|RW|WDC_BSL|DMA Base and Counter Lo                         |
$FFFF860E.B|RW|WDC_BSL|Frequency and Density control       %______FD |STE,F
           |  |        |Frequency 0:8MHz,1:16MHz--------------------+| |
           |  |        |Density 0:DD,1:HD---------------------------+ |
==========#==#=======#=================================================#=====
----------------------|DMA SCSI                                        |-----
==========#==#=======#=================================================#=====
$FFFF8701.B|RW|SCS_DA0|DMA Address Pointer (Highest byte)              |TT
```

```
$FFFF8703.B|RW|SCS_DA1|DMA Address Pointer (High byte)                |TT
$FFFF8705.B|RW|SCS_DA2|DMA Address Pointer (Low byte)                 |TT
$FFFF8707.B|RW|SCS_DA3|DMA Address Pointer (Lowest byte)              |TT
$FFFF8709.B|RW|SCS_BC0|DMA Byte Counter (Highest byte)                |TT
$FFFF870B.B|RW|SCS_BC1|DMA Byte Counter (High byte)                   |TT
$FFFF870D.B|RW|SCS_BC2|DMA Byte Counter (Low byte)                    |TT
$FFFF870F.B|RW|SCS_BC3|DMA Byte Counter (Lowest byte)                 |TT
$FFFF8710.W|Rw|SCS_DA0|Rest data (High Word)                          |TT
$FFFF8712.W|Rw|SCS_DA0|Rest data (Low Word)                           |TT
$FFFF8714.W|Rw|SCS_CTL|DMA SCSI Control Register   %_________ BZ____DW |TT
           |  |       | Bus Error 0:no,1:yes-----------------+|    || |TT
           |  |       | Byte Counter Zero 0:no,1:yes----------+    || |TT
           |  |       | DMA 0:off,1:on----------------------------+| |TT
           |  |       | DMA 0:read,1:write------------------------+ |TT
==========#==#=======#================================================#=====
----------------------|5380 SCSI Drive Controller                     |-----
==========#==#=======#================================================#=====
$FFFF8781.B|RW|SCS_CDB|Contents of SCSI-Data Buses                    |TT
$FFFF8783.B|RW|SCS_ICR|Init Command Register                          |TT
$FFFF8785.B|RW|SCS_TSR|Transfer Start Register                        |TT
$FFFF8787.B|RW|SCS_TCR|Target Command Register                        |TT
$FFFF8789.B|RW|SCS_BSR|Bus Status Register                           |TT
$FFFF878B.B|RW|SCS_DSR|Device Status Register                        |TT
$FFFF878D.B|RW|SCS_BCD|SCSI-Bus Command Data                         |TT
$FFFF878F.B|RW|SCS_RES|Reset Interupts,Parity error,Start DMA-Action  |TT
==========#==#=======#================================================#=====
----------------------|YM2149/AY-3-8910 Sound Chip                    |-----
==========#==#=======#================================================#=====
$FFFF8800.B|R-|PSG_SEL|Read Data                                      |
           |-W|       |Register Select                                |
$FFFF8802.B|rW|PSG_DAT|Write Data                                     |
           |  |       | PSG Register 14 - Port A           %RICDPBAS |
           |  |       | Reset IDE 0:no,1:reset (slow down)---+|||||| |F
           |  |       | Internal Speaker 0:on,1:off----------+|||||| |F
           |  |       | Centronics Strobe---------------------+||||| |
           |  |       | Reset DSP 0:no,1:reset-----------------+|||| |F
           |  |       | Printer Select In-----------------------+||| |
           |  |       | Drive B select 0:on,1:off----------------+|| |
           |  |       | Drive A select 0:on,1:off-----------------+| |
           |  |       | Side select 0:side1,1:side0----------------+ |
           |  |       | PSG Register 15 - Port B           %xxxxxxxx |
           |  |       | Centronics Data Port----------------++++++++ |
==========#==#=======#================================================#=====
----------------------|DMA,CODEC,ADC,DAC,DSP-Transmit,DSP-Receive     |-----
==========#==#=======#================================================#=====
$FFFF8900.W|RW|SND_DMA|Sound-DMA-Control          %____RPRP F_EL__EL |F,STE
           |  |       | Timer A after Record/Play-------++|| | ||  || |F
           |  |       | MFP I/O 7 after Record/Play-------++ | ||  || |F
           |  |       | Frame Registers 0:play,1:record------+ ||  || |F
           |  |       | DMA record Enable/Loop-----------------++  || |F
           |  |       | DMA play Enable/Loop----------------------++ |F,STE
$FFFF8903.B|RW|SND_FSH|Frame Start Hi                                 |F,STE
$FFFF8905.B|RW|SND_FSM|Frame Start Mi                                 |F,STE
$FFFF8907.B|RW|SND_FSL|Frame Start Lo                                 |F,STE
$FFFF8909.B|RW|SND_FCH|Frame Count Hi                                 |F,STE
$FFFF890B.B|RW|SND_FCM|Frame Count Mi                                 |F,STE
$FFFF890D.B|RW|SND_FCL|Frame Count Lo                                 |F,STE
$FFFF890F.B|RW|SND_FEH|Frame End Hi                                   |F,STE
$FFFF8911.B|RW|SND_FEM|Frame End Mi                                   |F,STE
$FFFF8913.B|RW|SND_FEL|Frame End Lo                                   |F,STE
$FFFF8920.W|RW|SND_SMC|Sound Mode Control         %__SS__PP MB____FF |F,STE
```

```
           |   |        | DAC to track %SS--------------++  || ||    || |F
           |   |        | Play %PP+1 tracks-----------------++ ||    || |F
           |   |        | 0:Stereo,0:Mono----------------------+|    || |F
           |   |        | 0:8bit,1:16bit-------------------------+    || |F
           |   |        | Falcon:nute------STE: 6258 Hz--------------00 |F,STE
           |   |        | Falcon:12292 Hz--STE:12517 Hz--------------01 |F,STE
           |   |        | Falcon:19668 Hz--STE:25033 Hz--------------10 |F,STE
           |   |        | Falcon:49170 Hz--STE:50066 Hz--------------11 |F,STE
$FFFF8922.B|RW|    -   |Microwire Data Register                        |STE
$FFFF8924.B|RW|    -   |Microwire Mask Register                        |STE
$FFFF8930.W|RW|SND_SDC|Source Device Clock         %_CC__CCH TCCHSCCH |F
           |   |        | A/D-Converter (%00 or %01)---++  ||| ||||||| |F
           |   |        | External Input------------------+++ ||||||| |F
           |   |        | 0:Tristate,1:connect DSP&Multiplexer-+||||||| |F
           |   |        | DSP Transmit-------------------------+++|||| |F
           |   |        | 0:if DMAplay->DSPrec and Handshake on----+||| |F
           |   |        | DMA Play---------------------------------+++ |F
           |   |        | 25.175 MHz Clock-------------------------00| |F
           |   |        | external Clock---------------------------01| |F
           |   |        | 32.000 MHz Clock-------------------------10| |F
           |   |        | nute-------------------------------------11| |F
           |   |        | Handshaking 0:on,1:off----------------------+ |F
$FFFF8932.W|RW|SND_DDM|Destination Device Matrix   %_DD__DDH TDDHSDDH |F
           |   |        | D/A-Converter----------------++  ||| ||||||| |F
           |   |        | External Output----------------+++ ||||||| |F
           |   |        | 0:Tristate,1:connect DSP&Multiplexer-+||||||| |F
           |   |        | DSP Receive-------------------------+++|||| |F
           |   |        | 0:if DMA Rec=%001-----------------------+||| |F
           |   |        | DMA Record--------------------------------+++ |F
           |   |        | Device:DMA Play--------------------------00+ |F
           |   |        | Device:DSP Transmit----------------------01+ |F
           |   |        | Device:External Input--------------------10+ |F
           |   |        | Device:A/D-Converter---------------------11+ |F
           |   |        | Handshaking 0:on,1:off----------------------+ |F
$FFFF8934.B|RW|SND_SEC|Scale External Clock                %____SSSS |F
$FFFF8935.B|RW|SND_SIC|Scale Internal Clock                %____SSSS |F
           |   |        | Clock/256  use Sound Mode Control--------0000 |F
           |   |        | Clock/512  (49170Hz)---------------------0001 |F
           |   |        | Clock/768  (32780Hz)---------------------0010 |F
           |   |        | Clock/1024 (24585Hz)---------------------0011 |F
           |   |        | Clock/1280 (19668Hz)---------------------0100 |F
           |   |        | Clock/1536 (16390Hz)---------------------0101 |F
           |   |        | Clock/1792 (14049Hz)-invalid-------------0110 |F
           |   |        | Clock/2048 (12292Hz)---------------------0111 |F
           |   |        | Clock/2304 (10927Hz)-invalid-------------1000 |F
           |   |        | Clock/2560 ( 9834Hz)---------------------1001 |F
           |   |        | Clock/2816 ( 8940Hz)-invalid-------------1010 |F
           |   |        | Clock/3072 ( 8195Hz)---------------------1011 |F
           |   |        | Clock/3328 ( 7565Hz)-invalid-------------1100 |F
           |   |        | Clock/3584 ( 7024Hz)-invalid-------------1101 |F
           |   |        | Clock/3840 ( 6556Hz)-invalid-------------1110 |F
           |   |        | Clock/4096 ( 6146Hz)-invalid-------------1111 |F
$FFFF8936.B|RW|SND_TRC|Track Record Control                 %______TT |F
           |   |        | Record %TT+1 Tracks                          |F
$FFFF8937.B|RW|SND_CDI|CODEC Input                          %______MA |F
           |   |        | A/D-Converter 0:dis-,1:connect-------------+| |F
           |   |        | Multiplexer 0:dis-,1:connect with CODEC-----+ |F
$FFFF8938.B|RW|SND_ADC|A/D-Converter Input                  %______LR |F
           |   |        | 0:External Input (left/right),1:PSG--------++ |F
$FFFF8939.B|RW|SND_CIA|Channel Input Amplifier             %LLLLRRRR |F
$FFFF893A.W|RW|SND_COR|Channel Output Reduction    %____LLLL RRRR____ |F
```

```
$FFFF893C.W|Rw|SND_CDS|CODEC Status                %______LR LR______ |F
           |  |       | Overflow left/rigth--------------++ ||       |F
           |  |       | Overrun left/rigth-------------------++       |F
$FFFF8940.W|RW|SND_DIR|GPx Dircetion               %_________ _____GGG |F
           |  |       | G0-G2 Pin 0:input,1:output----------------+++ |F
$FFFF8942.W|RW|SND_PRT|GPx Port                    %_____GGG _____GGG |F
           |  |       | G0-G2 Pin input/output-----------+++------+++ |F
===========#==#=======#================================================#=====
----------------------|Realtime Clock Chip, Non Volatile Memory       |-----
===========#==#=======#================================================#=====
$FFFF8961.B|RW|NVM_CTL|Register Select                                 |TT,F
$FFFF8963.B|RW|NVM_DAT|Data of selected Register                      |TT,F
===========#==#=======#================================================#=====
----------------------|DMA,Blitter                                    |-----
===========#==#=======#================================================#=====
$FFFF8A00.W|RW|BLT_HTR|Halftone-Ram 00                                 |BLT
...........|RW|   -   |.............                                  |BLT
$FFFF8A1E.W|RW|   -   |Halftone-Ram 15                                 |BLT
$FFFF8A20.W|RW|BLT_SXI|Source X increment          %xxxxxxxx xxxxxxx_ |BLT
$FFFF8A22.W|RW|BLT_SYI|Source Y increment          %xxxxxxxx xxxxxxx_ |BLT
$FFFF8A24.L|RW|BLT_SRC|Source Address     %xxxxxxxx xxxxxxxx xxxxxxx_ |BLT
$FFFF8A28.W|RW|BLT_EM1|Endmask 1                                       |BLT
$FFFF8A2A.W|RW|BLT_EM2|Endmask 2                                       |BLT
$FFFF8A2C.W|RW|BLT_EM3|Endmask 3                                       |BLT
$FFFF8A2E.W|RW|BLT_DXI|Destination X increment     %xxxxxxxx xxxxxxx_ |BLT
$FFFF8A30.W|RW|BLT_DYI|Destination Y increment     %xxxxxxxx xxxxxxx_ |BLT
$FFFF8A32.L|RW|BLT_DST|Destination Adr.   %xxxxxxxx xxxxxxxx xxxxxxx_ |BLT
$FFFF8A36.W|RW|BLT_WPL|Words per Line in BOB                (0:65536)|BLT
$FFFF8A38.W|RW|BLT_LPB|Lines per BOB                        (0:65536)|BLT
$FFFF8A3A.B|RW|BLT_HTO|Halftone Operation                  %______xx |BLT
           |  |       | 0:set all Bits, 1:HTR, 2:SRC, 3:SRC & HTR     |BLT
$FFFF8A3B.B|RW|BLT_LGO|Logical Operation                   %____xxxx |BLT
           |  |       | (!S AND !D)-----------------------------+||| |BLT
           |  |       | (!S AND  D)------------------------------+|| |BLT
           |  |       | ( S AND !D)-------------------------------+| |BLT
           |  |       | ( S AND  D)--------------------------------+ |BLT
$FFFF8A3C.B|RW|BLT_LNM|Line Number                          %BHS_xxxx |BLT
           |  |       | Busy (1:start Blitter)---------------+|| |||| |BLT
           |  |       | HOG (1:stop CPU when Busy)------------+| |||| |BLT
           |  |       | SMUDGE (use sourcebits 0-3 as HTR num)-+ |||| |BLT
           |  |       | Halftone-Ram number----------------------++++ |BLT
$FFFF8A3D.B|RW|BLT_SKW|SKEW                                  %FN__xxxx |BLT
           |  |       | FXSR (Force eXtra Source Read)-------+|  |||| |BLT
           |  |       | NFSR (No Final Source Read)-----------+  |||| |BLT
           |  |       | SKEW (shift)-----------------------------++++ |BLT
===========#==#=======#================================================#=====
----------------------|DMA SCC                                        |-----
===========#==#=======#================================================#=====
$FFFF8C01.B|RW|SCC_DA0|DMA Address Pointer (Highest byte)              |TT
$FFFF8C03.B|RW|SCC_DA1|DMA Address Pointer (High byte)                 |TT
$FFFF8C05.B|RW|SCC_DA2|DMA Address Pointer (Low byte)                  |TT
$FFFF8C07.B|RW|SCC_DA3|DMA Address Pointer (Lowest byte)               |TT
$FFFF8C09.B|RW|SCC_BC0|DMA Byte Counter (Highest byte)                |TT
$FFFF8C0B.B|RW|SCC_BC1|DMA Byte Counter (High byte)                   |TT
$FFFF8C0D.B|RW|SCC_BC2|DMA Byte Counter (Low byte)                    |TT
$FFFF8C0F.B|RW|SCC_BC3|DMA Byte Counter (Lowest byte)                 |TT
$FFFF8C10.W|Rw|SCC_DA0|Rest data (High Word)                          |TT
$FFFF8C12.W|Rw|SCC_DA0|Rest data (Low Word)                           |TT
$FFFF8C14.W|Rw|SCC_CTL|DMA SCC Control Register    %_________ BZ____DW |TT
           |  |       | Bus Error 0:no,1:yes-----------------+|    || |TT
           |  |       | Byte Counter Zero 0:no,1:yes----------+    || |TT
```

```
          |  |       | DMA 0:off,1:on-----------------------------+| |TT
          |  |       | 0:DMA read,1:DMA write---------------------+ |TT
==========#==#=======#================================================#=====
----------------------|SCC Y8530 - Serial Communication Controller    |-----
==========#==#=======#================================================#=====
$FFFF8C81.B|RW|SCA_CTL|Channel A Control (select/read/write Register) |SCC
$FFFF8C83.B|RW|SCA_DAT|Channel A Data    (read/write Register 8)      |SCC
$FFFF8C85.B|RW|SCB_CTL|Channel B Control (select/read/write Register) |SCC
$FFFF8C87.B|RW|SCB_DAT|Channel B Data    (read/write Register 8)      |SCC
==========#==#=======#================================================#=====
----------------------|VME Bus                                        |-----
==========#==#=======#================================================#=====
$FFFF8E01.B|RW|VME_MR0|VME Mask Register 0                            |TT,ME
$FFFF8E03.B|RW|VME_SR0|VME Status Register 0               %EMSV_HS_ |TT,ME
          |  |       | Error 0:no,1:yes--------------------+||| ||  |TT,ME
          |  |       | MFP----------------------------------+|| ||  |TT,ME
          |  |       | SCC-----------------------------------+| ||  |TT,ME
          |  |       | VBL------------------------------------+ ||  |TT,ME
          |  |       | HBL-------------------------------------+|  |TT,ME
          |  |       | Software Intereupt-----------------------+  |TT,ME
$FFFF8E05.B|RW|VME_IN0|Force Interrupt on Level 1          %_______F |TT,ME
$FFFF8E07.B|RW|VME_IN1|Force Interrupt on Level 3          %_______F |TT,ME
$FFFF8E0D.B|RW|VME_MR1|VME Mask Register 1                           |TT,ME
$FFFF8E0F.B|RW|VME_SR1|VME Status Register 1               %7654321_ |TT,ME
          |  |       | VME Interrupt 1-7 0:on,1:off--------+++++++  |
----------+--+-------+-------------------------------------------+-----
$FFFF8E0F.B|RW|M_E_CAC|Cache and CPU Control                %???????? |ME
==========#==#=======#================================================#=====
----------------------|Paddle Ports                                   |-----
==========#==#=======#================================================#=====
$FFFF9200.W|RW|PAD_BUT|Paddle/Joy Buttons          %xxxxxxxx ____3210 |STE,F
          |  |       | Switches--------------------++++++++          |,TT
          |  |       | On Falcon at U47: MSB on the rigth,closed=0   |
$FFFF9202.W|RW|PAD_MOV|Paddle/Joy Move                               |STE,F
$FFFF9210.W|RW|PAD_PD0|Pad0 Position                                 |STE,F
$FFFF9212.W|RW|PAD_PD1|Pad1 Position                                 |STE,F
$FFFF9214.W|RW|PAD_PD2|Pad2 Position                                 |STE,F
$FFFF9216.W|RW|PAD_PD3|Pad3 Position                                 |STE,F
$FFFF9220.W|RW|PAD_LPX|Lightpen X                                    |STE,F
$FFFF9222.W|RW|PAD_LPY|Lightpen Y                                    |STE,F
==========#==#=======#================================================#=====
----------------------|VIDEL Pallete Register                         |-----
==========#==#=======#================================================#=====
$FFFF9800.L|RW|VDL_PAL|Pallete Register 000        %RRRRRR__ GGGGGG__ |F
...........|RW|   -   |.....................        _________ BBBBBB__ |F
$FFFF98FC.L|RW|   -   |Pallete Register 255                           |F
==========#==#=======#================================================#=====
----------------------|DSP 56001 Host - Digital Sync Processor        |-----
==========#==#=======#================================================#=====
$FFFFA200.B|RW|DSP_ICR|Intrrupt Control Register (%IMMHH_TR)          |DSP
$FFFFA201.B|RW|DSP_CVR|Command Vector Register   (%I__VVVVV)          |DSP
$FFFFA202.B|RW|DSP_ISR|Interrupt Status Register (%ID_HHETR)          |DSP
$FFFFA203.B|RW|DSP_IVR|Interrupt Vector Register (Vector Number)      |DSP
$FFFFA204.B|RW|DSP_TR0|Transfer Highest Byte (DSP56003 32bit)        |DSP32
$FFFFA205.B|RW|DSP_TR1|Transfer Hi                                    |DSP
$FFFFA206.B|RW|DSP_TR2|Transfer Mi                                    |DSP
$FFFFA207.B|RW|DSP_TR3|Transfer Lo                                    |DSP
==========#==#=======#================================================#=====
----------------------|MFP 68901 - Multi Function Peripheral          |-----
==========#==#=======#================================================#=====
$FFFFFA01.B|RW|MFP_PDR|Paralellport Data Register          %SRFKBRDC |
```

```
$FFFFFA03.B|RW|MFP_AER|Aktive Edge Register                  %SRFKBRDC |
           |  |       | Interrupt on 0:High-Low,1:Low-High   ||||||||  |!F
           |  |       | Interrupt on 0:Low-High,1:High-Low   ||||||||  |F
$FFFFFA05.B|RW|MFP_DIR|Data-direction                        %SRFKBRDC |
           |  |       | I/O-7 Mono Detect/Sound-------------+|||||||  |
           |  |       | I/O-6 RS232 Ring Indicator-----------+||||||  |
           |  |       | I/O-5 FDC/HDC-------------------------+|||||  |
           |  |       | I/O-4 IKBD/MIDI-----------------------+||||  |
           |  |       | I/O-3 Blitter Done---------------------+|||  |
           |  |       | I/O-2 RS232 CTS-----------------------+||  |
           |  |       | I/O-1 RS232 DCD-----------------------+|  |
           |  |       | I/O-0 Centronics Busy-----------------+  |
$FFFFFA07.B|RW|MFP_IEA|Interrupt Enable A                    %76AbebeB |
$FFFFFA09.B|RW|MFP_IEB|Interrupt Enable B                    %54CD3210 |
$FFFFFA0B.B|RW|MFP_IPA|Interrupt Pending A                   %76AbebeB |
$FFFFFA0D.B|RW|MFP_IPB|Interrupt Pending B                   %54CD3210 |
$FFFFFA0F.B|RW|MFP_ISA|Interrupt In-Service A                %76AbebeB |
$FFFFFA11.B|RW|MFP_ISB|Interrupt In-Service B                %54CD3210 |
$FFFFFA13.B|RW|MFP_IMA|Interrupt Mask A                      %76AbebeB |
           |  |       | I/O 7 Mono Detect/Sound-------------+|||||||  |
           |  |       | I/O 6 RS232 Ring---------------------+||||||  |
           |  |       | Timer A-------------------------------+|||||  |
           |  |       | Receive Buffer full-------------------+||||  |
           |  |       | Receive Error-----------------------------+|||  |
           |  |       | Transmit Buffer empty---------------------+||  |
           |  |       | Transmit Error-----------------------------+|  |
           |  |       | Timer B-------------------------------------+  |
$FFFFFA15.B|RW|MFP_IMB|Interrupt Mask B                      %54CD3210 |
           |  |       | I/O 5 FDC/HDC-----------------------+|||||||  |
           |  |       | I/O 4 IKBD/MIDI---------------------+||||||  |
           |  |       | Timer C-------------------------------+|||||  |
           |  |       | Timer D-------------------------------+||||  |
           |  |       | I/O 3 Blitter Done---------------------+|||  |
           |  |       | I/O 2 RS232 CTS-----------------------+||  |
           |  |       | I/O 1 RS232 DCD-----------------------+|  |
           |  |       | I/O 0 Centronics Busy-----------------+  |
$FFFFFA17.B|RW|MFP_VCR|Vector Register                       %xxxxI___ |0100
           |  |       | End of Interupt 0:software,1:auto--------+    |1000
           |  |       | VCR should contain------------------%0100?000 |*
$FFFFFA19.B|RW|MFP_TAC|Timer A Control                       %____EAAA |
$FFFFFA1B.B|RW|MFP_TBC|Timer B Control                       %____EBBB |
           |  |       | Event Count Mode------------------------1000  |
           |  |       | Pulse Extension-------------------------1xxx  |
           |  |       | Delay-----------------------------------0xxx  |
           |  |       |                                          |||  |
$FFFFFA1D.B|RW|MFP_TDC|Timer C+D Control                     %_CCC_DDD |
           |  |       | Timer C Control----------------------+++ |||  |
           |  |       | Timer D Control-----------------------------+++  |
           |  |       | Stop Timer--------------------------------000  |
           |  |       | Delay,Clockdivide   4 3200Hz-------------001  |
           |  |       | Delay,Clockdivide  10 1280Hz-------------010  |
           |  |       | Delay,Clockdivide  16  800Hz-------------011  |
           |  |       | Delay,Clockdivide  50  256Hz-------------100  |
           |  |       | Delay,Clockdivide  64  200Hz-------------101  |
           |  |       | Delay,Clockdivide 100  128Hz-------------110  |
           |  |       | Delay,Clockdivide 200   64Hz-------------111  |
$FFFFFA1F.B|RW|MFP_TAD|Timer A Data                                   |
$FFFFFA21.B|RW|MFP_TBD|Timer B Data                                   |
$FFFFFA23.B|RW|MFP_TCD|Timer C Data                                   |
$FFFFFA25.B|RW|MFP_TDD|Timer D Data                                   |
$FFFFFA27.B|RW|MFP_SYC|Syncronous Character                         |
```

```
$FFFFFA29.B|RW|MFP_UCR|Usart Control                          %DBBSSPE_ |
           |  |       | Divider 0:div1(sync),1:div16---------+|||||  |
           |  |       | Databits 00:8,01:7,10:6,11:5----------++||||  |
           |  |       | 00:sync,01:1stop,10:1.5stop,11:2stop----++||  |
           |  |       | Parity 0:off,1:on-------------------------+|  |
           |  |       | Parity 0:odd,1:even------------------------+  |
$FFFFFA2B.B|RW|MFP_RES|Receiver Status                       %BOPFSCPR |
           |  |       | Buffer full--------------------------+|||||| |
           |  |       | Overrun Error------------------------+|||||| |
           |  |       | Parity Error-------------------------+||||| |
           |  |       | Frame Error--------------------------+|||| |
           |  |       | SCR found/Break----------------------+||| |
           |  |       | SCR received/Startbit detected-------+|| |
           |  |       | Syncronous Strip Enable--------------+| |
           |  |       | Receiver Enable----------------------+ |
$FFFFFA2D.B|RW|MFP_TRS|Transmitter Status                     %BUAEBHLT |
           |  |       | Buffer Empty-------------------------+||||||| |
           |  |       | Underrun Error (char sent)-----------+|||||| |
           |  |       | Auto Turnaround----------------------+||||| |
           |  |       | EOT End of Transmission--------------+|||| |
           |  |       | Break--------------------------------+||| |
           |  |       | 00:High,01:Low,10:High,11:loopback,High---++| |
           |  |       | Transmitter Enable-------------------------+ |
$FFFFFA2F.B|RW|MFP_UAD|Usart Data                                    |
===========#==#=======#==============================================#=====
----------------------|FPC - Floating Point Coprocessor              |-----
===========#==#=======#==============================================#=====
$FFFFFA40.W|RW|FPC_STA|Status Register                                |ME
$FFFFFA42.W|RW|FPC_CTL|Cotrol Register                               |ME
$FFFFFA44.W|RW|FPC_SAV|Save Register                                 |ME
$FFFFFA46.W|RW|FPC_RES|Restore Register                              |ME
$FFFFFA4A.W|RW|FPC_CMD|Command Register                              |ME
$FFFFFA4E.W|RW|FPC_CCR|Conditional Code Register                     |ME
$FFFFFA46.W|RW|FPC_OPR|Operand Register                              |ME
$FFFFFA46.W|RW|FPC_IAR|Instruction Address Register                  |ME
===========#==#=======#==============================================#=====
----------------------|MFP 68901 number 2                            |-----
===========#==#=======#==============================================#=====
$FFFFFA81.B|RW|MF2_PDR|Parallel Port Data Register                   |TT
...........|  |       |.........................                     |TT
$FFFFFAAF.B|RW|MF2_PDR|USART Data Register                           |TT
===========#==#=======#==============================================#=====
----------------------|ACIA 6850 (Midi/Keyboard)                     |-----
===========#==#=======#==============================================#=====
$FFFFFC00.B|R-|KBD_CTL|IKBD Status                           %IPOFCDTR |
     "     |-W|KBD_CTL|IKBD Control                          %ITTBSPDD |
           |  |       | 7N1,7812.5,RTS low,Rec on,Send off= %10010110 |*
$FFFFFC02.B|RW|KBD_DAT|IKBD Data                                      |
$FFFFFC04.B|R-|MID_CTL|MIDI Status                           %IPOFCDTR |
           |  |       | Interrupt Request--------------------+||||||| |
           |  |       | Parity Error-------------------------+|||||| |
           |  |       | Receiver Overrun---------------------+||||| |
           |  |       | Frame Error--------------------------+|||| |
           |  |       | CTS Clear to Send--------------------+||| |
           |  |       | DCD Data Carrier Detect--------------+|| |
           |  |       | Transmitter Data Register full-------+| |
           |  |       | Receiver Data Register full----------+ |
     "     |-W|MID_CTL|MIDI Control                          %ITTBSPDD |
           |  |       | 7N1,31250,RTS low,Rec on,Send off = %10010101 |*
           |  |       | Interrupt 0:off,1:on----------------+||||||| |
           |  |       | RTS low, TransmitIRQ off-----------00||||| |
```

```
           |  |       | RTS low, TransmitIRQ on---------------01|||||  |
           |  |       | RTS high,TransmitIRQ off--------------10|||||  |
           |  |       | RTS low, TransmitIRQ off,send break---11|||||  |
           |  |       | 8 Databits,2 Stopbits,Parity even-------000||  |
           |  |       | 8 Databits,2 Stopbits,Parity odd--------001||  |
           |  |       | 8 Databits,1 Stopbits,Parity even-------010||  |
           |  |       | 8 Databits,1 Stopbits,Parity odd--------011||  |
           |  |       | 7 Databits,2 Stopbits,Parity off--------100||  |
           |  |       | 7 Databits,1 Stopbits,Parity off--------101||  |
           |  |       | 7 Databits,1 Stopbits,Parity even-------110||  |
           |  |       | 7 Databits,1 Stopbits,Parity odd--------111||  |
           |  |       | Clockdivide  1 - 500000.0cps---------------00  |
           |  |       | Clockdivide 16 -  31250.0cps (MIDI Std)----01  |
           |  |       | Clockdivide 64 -   7812.5cps (IKBD!)-------10  |
           |  |       | Master Reset-------------------------------11  |
           |  |       | To link per MIDI you can also use div1/div64!  |
$FFFFFC06.B|RW|MID_DAT|MIDI Data                                       |
===========#==#=======#================================================#=====
----------------------|RP5C15 Real Time Clock                          |-----
===========#==#=======#================================================#=====
$FFFFFC21.B|RW|   -   |Seconds mod 10                      %____xxxx |MST
$FFFFFC23.B|RW|   -   |Seconds div 10                      %____xxxx |MST
$FFFFFC25.B|RW|   -   |Minutes mod 10                      %____xxxx |MST
$FFFFFC27.B|RW|   -   |Minutes div 10                      %____xxxx |MST
$FFFFFC29.B|RW|   -   |Hours mod 10                        %____xxxx |MST
$FFFFFC2B.B|RW|   -   |Hours div 10                        %____xxxx |MST
$FFFFFC2D.B|RW|   -   |Weekday                             %____xxxx |MST
$FFFFFC2F.B|RW|   -   |Day mod 10                          %____xxxx |MST
$FFFFFC31.B|RW|   -   |Day div 10                          %____xxxx |MST
$FFFFFC33.B|RW|   -   |Month mod 10                        %____xxxx |MST
$FFFFFC35.B|RW|   -   |Month div 10                        %____xxxx |MST
$FFFFFC37.B|RW|   -   |Year mod 10                         %____xxxx |MST
$FFFFFC39.B|RW|   -   |Year div 10                         %____xxxx |MST
$FFFFFC3B.B|RW|   -   |Clock mod                           %____xxxx |MST
$FFFFFC3D.B|RW|   -   |Clock test                          %____xxxx |MST
$FFFFFC3F.B|RW|   -   |Clock reset                         %____xxxx |MST
===========#==#=======#================================================#=====
$FFFFFF82.W|RW|       |
===========#==#=======#================================================#=====
$FFFF820D.B|RW|VDL_VBL|Video Base Lo                        %xxxxxxx_ |STE,F
----+----  | +- ---+--- ------------------+---------------------------- --+--
    |      | |     |                      |                               |
    |      | |     |                      |   Computer Type---------------+
    |      | |     |                      +---Description
    |      | |     +--------------------------Label
    |      | +--------------------------------Read/Write Access
    |      +----------------------------------Type (Byte,Word,Long)
    +-----------------------------------------Address (extended to 32 Bit)
Computer Type:
*   |Software defined Standart
!xxx|all except xxx
0x0 |MC680x0 only
0x0+|MC680x0 or higher
BLT |Standart on TT,STE,ME,F (Blitter)
SCC |Standart on TT,ME,F
VME |Standart on TT,ME
ST  |Atari ST  (260/520/1040)
STE |Atari STE (520/1040)
TT  |Atari TT
MST |Atari Mega ST (1/2)
ME  |Atari Mega STE
```

```
F   |Atari Falcon

Description:
%

Read/Write Access:
R/-|Read only (Readregister)
-/W|Write only (Writeregister)
R/?|Readaccess allowed
?/W|Writeaccess allowed
r/?|Readaccess allowed but not senseful
?/w|Writeaccess allowed but not senseful
```