APPENDIX B
APPLICATION EXAMPLES

The lowest cost DSP56001 based system is shown in Figure B-1. It uses no run time external memory and requires only two chips, the DSP56001 and a low cost EPROM. The EPROM read access time should be less than 780 nanoseconds when the DSP56001 is operating at a clock rate of 20.5 MHz.

A system with external data RAM memory requires no glue logic to select the external EPROM from bootstrap mode. $\overline{PS}$ is used to enable the EPROM and $\overline{DS}$ is used to enable the high speed data memories as shown in Figure B-2.

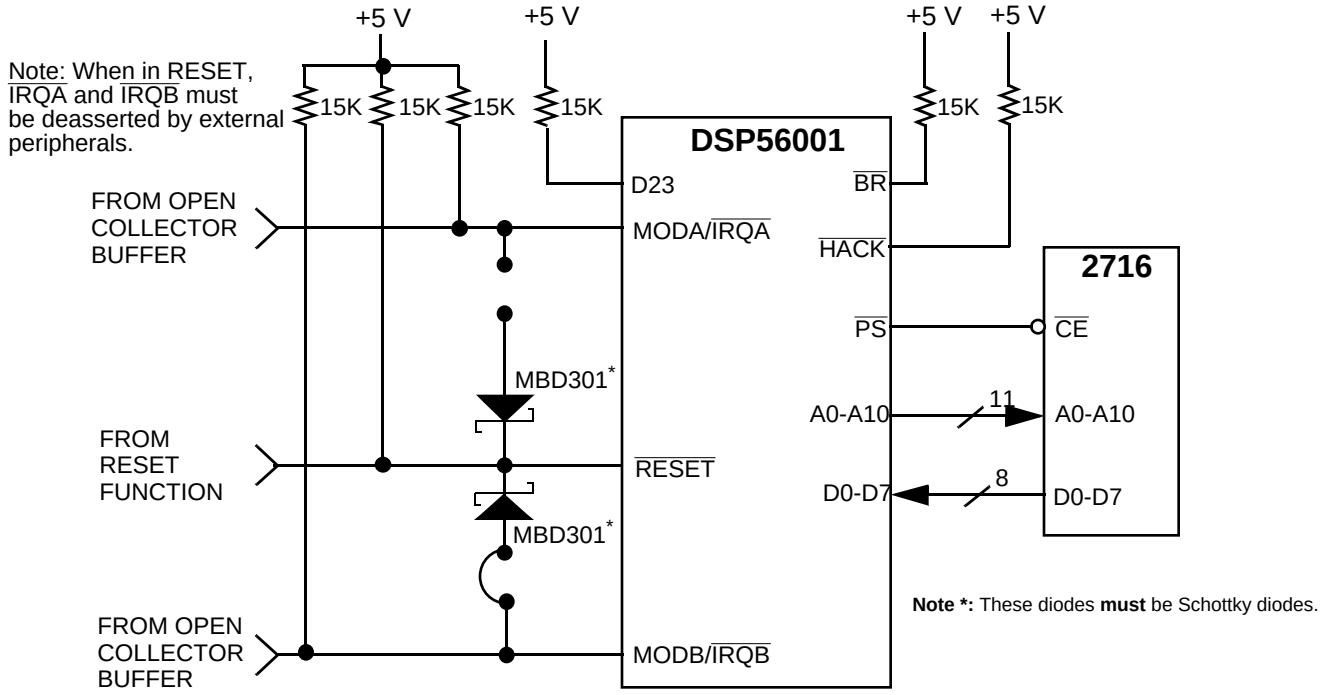


Figure B-1. No Glue Logic, Low Cost Memory Port Bootstrap — Mode 1

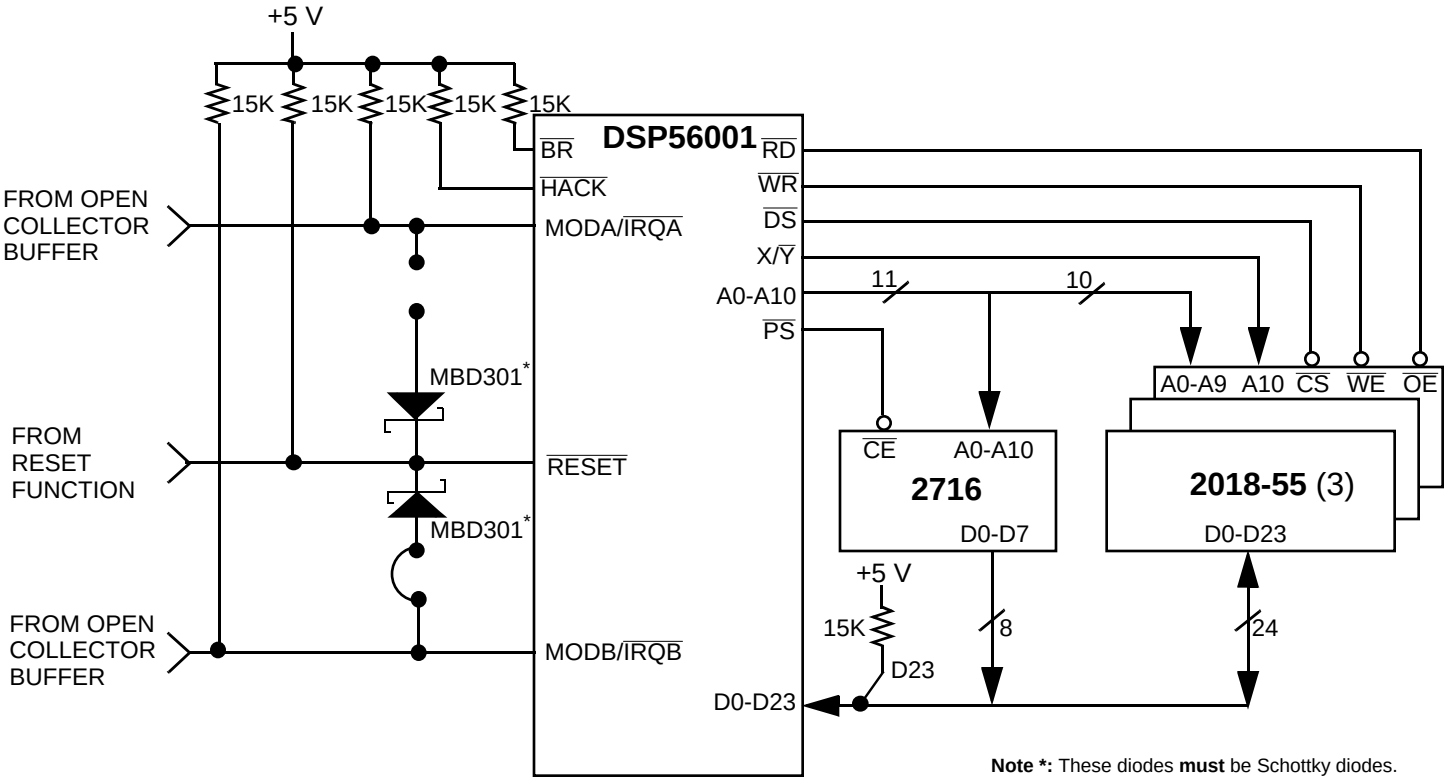


Figure B-2. Port A Bootstrap with External Data RAM — Mode 1

Figure B-3 shows the DSP56001 bootstrapping via the Host Port from an MC68000.

Systems with external program memory can load the on-chip PRAM without using the bootstrap mode. In Figure B-4, the DSP56001 is operated in mode 2 with external program memory at location $E000. The programmer can overlay the high speed on-chip PRAM with DSP algorithms by using the MOVEM instruction.

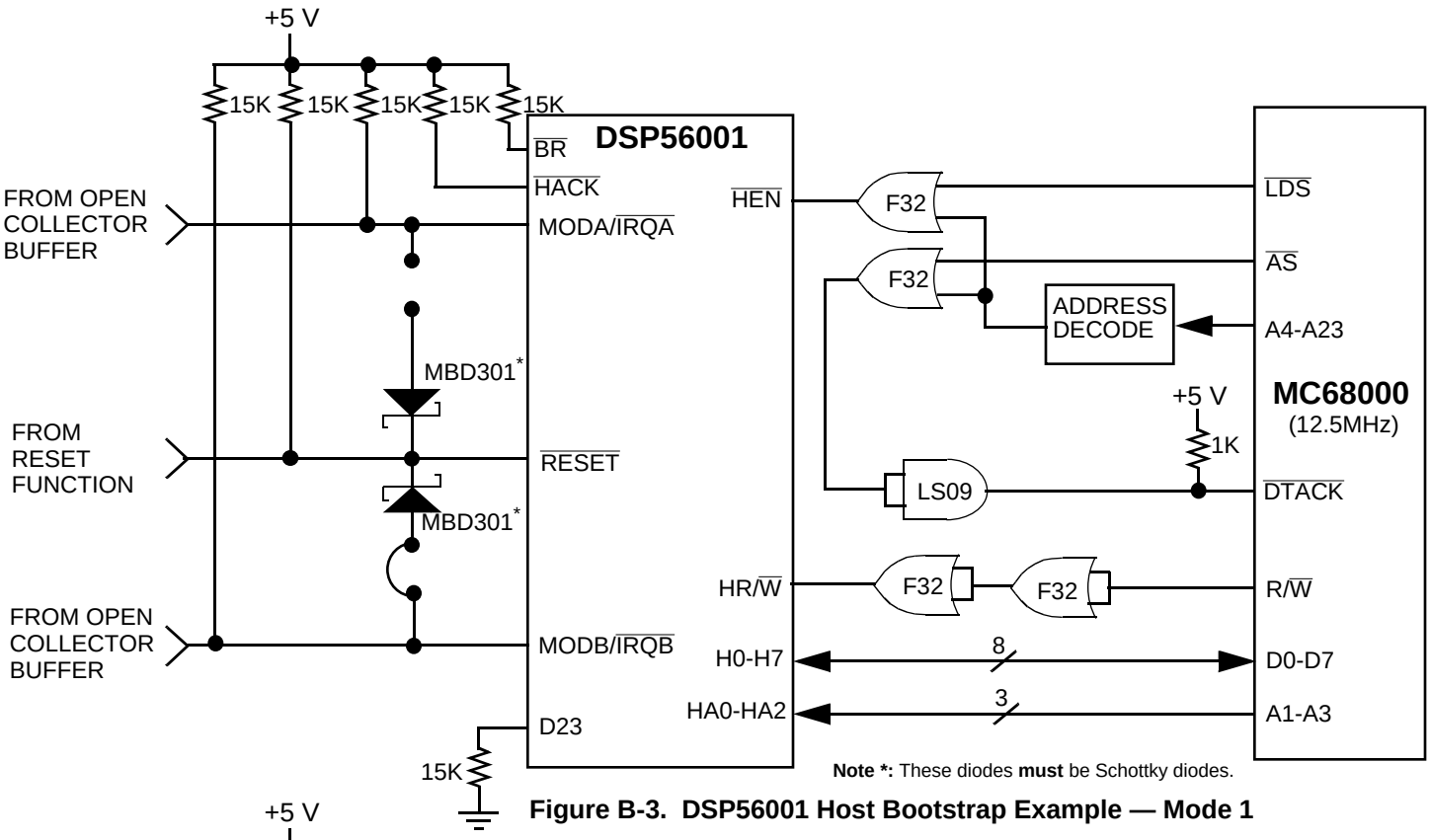


Figure B-3. DSP56001 Host Bootstrap Example — Mode 1

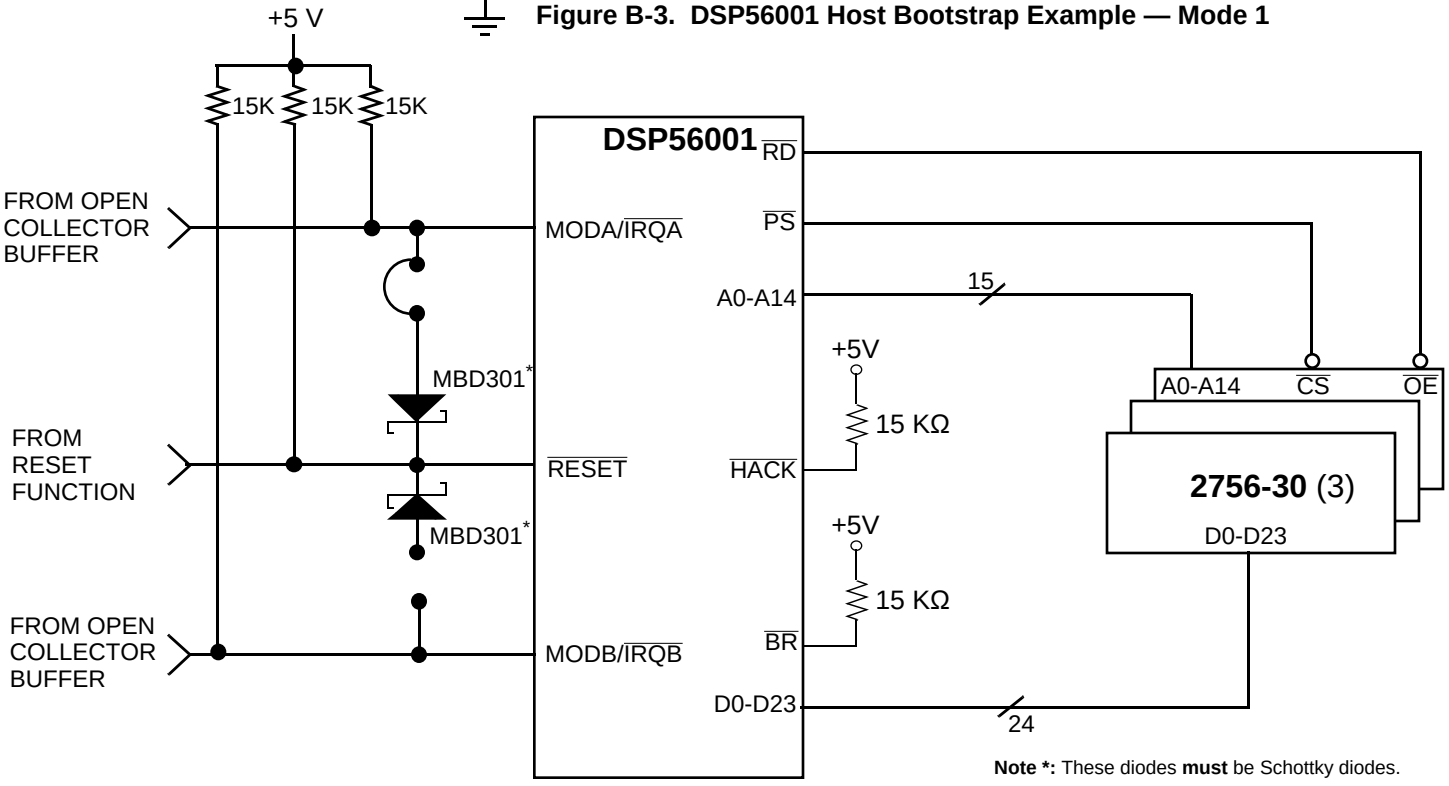


Figure B-4. 32K Words of External Program ROM — Mode 2

Figure B-5 shows an alternative clock oscillator circuit used in the Graphic Equalizer application note (APR2). The 330Ω resistor provides additional current limiting in the crystal. Figure B-6 shows a circuit which waits until Vcc on the DSP is at least 4.5 V before initiating a 3.75 ms minimum (150,000T) oscillator stabilization delay required for the on-chip oscillator (only 50T is required for an external oscillator). This insures that the DSP is operational and stable before releasing the reset signal.

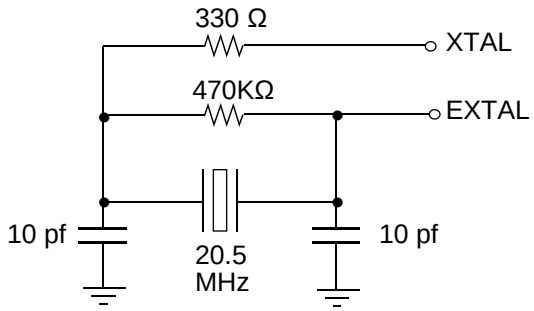
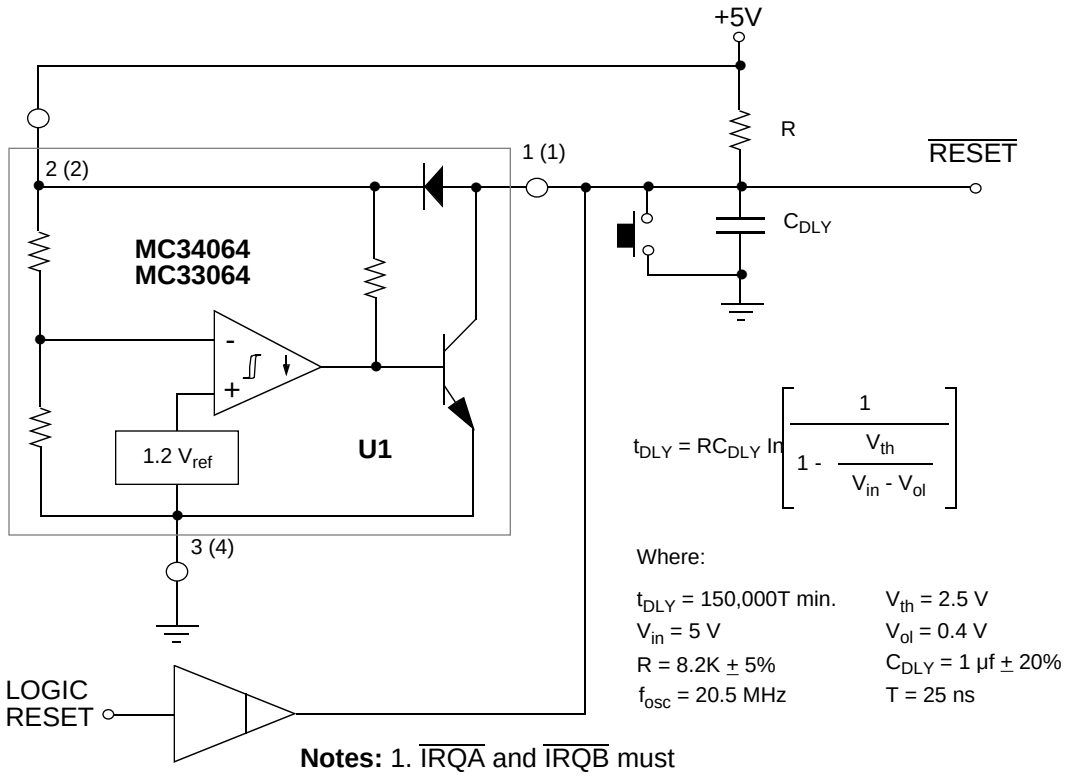


Figure B-5. Alternative Clock Circuit from the Graphic Equalizer (APR2)



Notes: 1. $\overline{\text{IRQA}}$ and $\overline{\text{IRQB}}$ must be hardwired.

2. MODA and MODB must be hard wired.

Figure B-6. Reset Circuit Using MC34064/MC33064

Figure 7 illustrates how to connect a 20 ns static RAM with a 33 MHz. DSP56001. The important parameters are $T_{DW} \leq 10$ ns, $T_{DOE} \leq 10$ ns, and $T_{AA} = 20$ ns maximum. A 7.5 ns PLD is used to minimize decoding delays. This example maps the static RAM into the ranges X:$1000-1FFF and Y:$1000-1FFF. The PLD equation is:

$\overline{RAM\_ENABLE} = \overline{PS}$ & !$\overline{DS}$ & !A15 & !A14 & !A13 & !A12

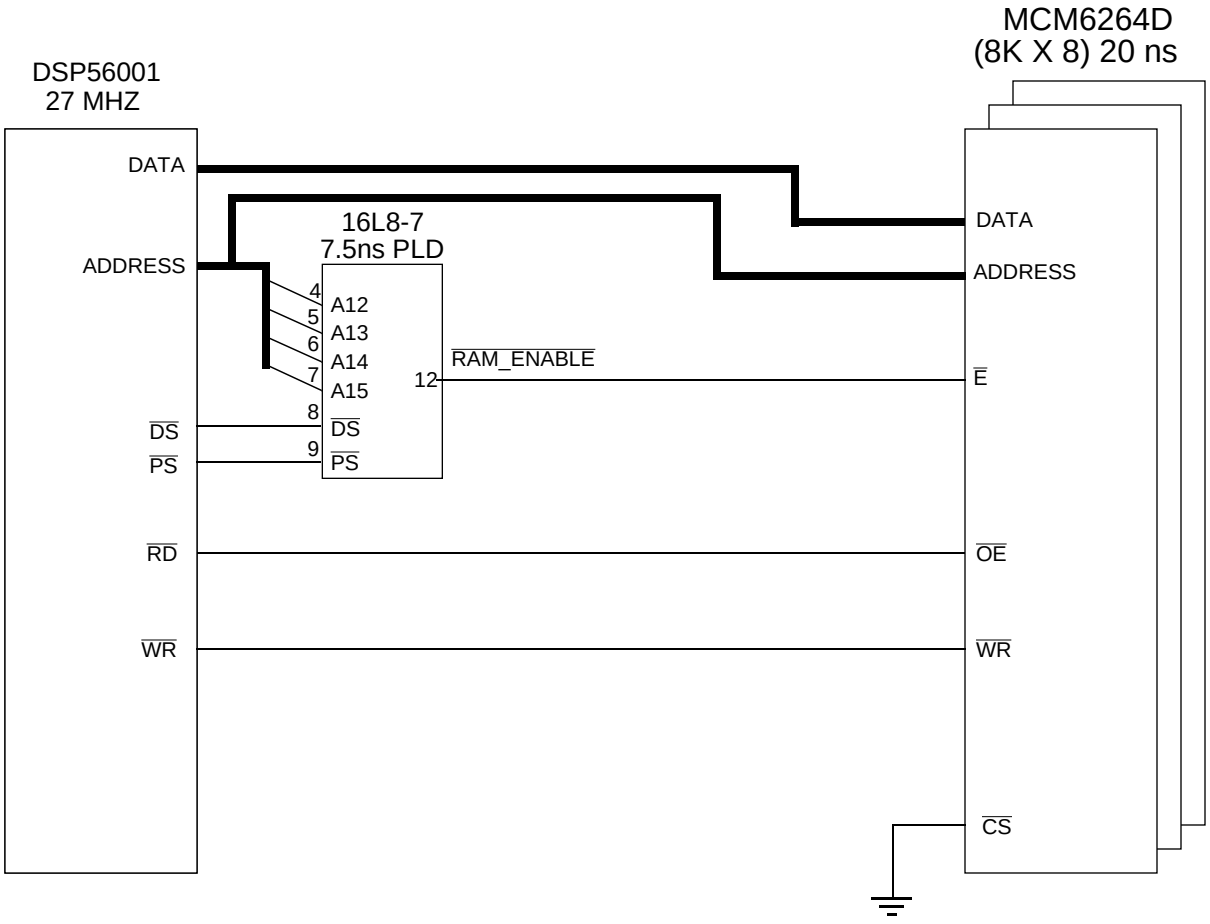


Figure B-7. 27 MHz DSP56001 with 20 ns SRAM

Figure B-8 shows the DSP56001 connected to the bus of an IBM-PC computer. The PAL equations and other details of this circuit are available in “An ISA BUS INTERFACE FOR THE DSP56001” which is provided on request by the Motorola DSP Marketing Department (512-891-2030).

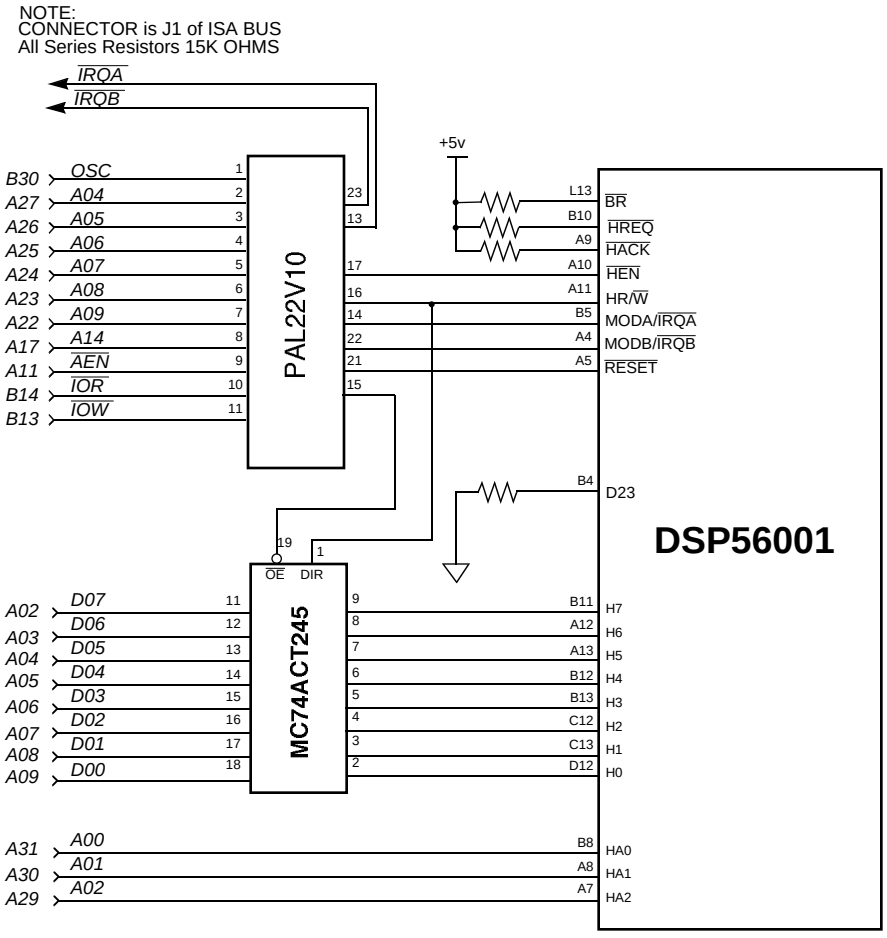


Figure B-8. DSP56001-to-ISA Bus Interface Schematic