DSP56001 Electrical Characteristics
Electrical Specifications

The DSP is fabricated in high density CMOS with TTL compatible inputs and outputs.

Maximum Ratings (V_{SS} = 0 Vdc)

Rating	Symbol	Value	Unit
Supply Voltage	Vcc	-0.3 to +7.0	V
All Input Voltages	Vin	V_{SS}- 0.5 to Vcc + 0.5	V
Current Drain per Pin excluding Vcc and V_{SS}	I	10	mA
Operating Temperature Range	T_J	-40 to +105	°C
Storage Temperature	Tstg	-55 to +150	°C

Maximum Electrical Ratings

Thermal Characteristics - PGA Package

Characteristics Thermal Resistance - Ceramic	Symbol	Value	Rating
Junction to Ambient Junction to Case (estimated)	Θ_{JA} Θ_{JC}	27 6.5	°C/W °C/W

Thermal Characteristics - CQFP Package

Characteristics Thermal Resistance - Ceramic	Symbol	Value	Rating
Junction to Ambient Junction to Case (estimated)	Θ_{JA} Θ_{JC}	40 7.0	°C/W °C/W

Thermal Characteristics - PQFP Package

Characteristics Thermal Resistance - Plastic	Symbol	Value	Rating
Junction to Ambient Junction to Case (estimated)	Θ_{JA} Θ_{JC}	38 13.0	°C/W °C/W

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either Gnd or Vcc).

Power Considerations

The average chip-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

Θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{CC} \times Vcc$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins - User Determined

For most applications $P_{I/O} << P_{INT}$ and can be neglected; however, $P_{I/O} + P_{INT}$ **must not** exceed P_d. An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K/(T_J + 273° C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273° C) + \Theta_{JA} \times P_D^2 \quad (3)$$

Where K is a constant pertaining to the particular part. K can be determined from equation (2) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A. The total thermal resistance of a package (Θ_{JA}) can be separated into two components, Θ_{JC} and C_A, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (Θ_{JC}) and from the case to the outside ambient (C_A). These terms are related by the equation:

$$\Theta_{JA} = \Theta_{JC} + C_A \quad (4)$$

Θ_{JC} is device related and cannot be influenced by the user. However, C_A is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce C_A so that Θ_{JA} approximately equals Θ_{JC}. Substitution of Θ_{JC} for Θ_{JA} in equation (1) will result in a lower semiconductor junction temperature. Values for thermal resistance presented in this document, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, “Thermal Resistance Measurement Method for MC68XX Microcomponent Devices”, and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

Layout Practices

Each Vcc pin on the DSP56001 should be provided with a low-impedance path to + 5 volts. Each GND pin should likewise be provided with a low-impedance path to ground. The power supply pins drive four distinct groups of logic on chip. They are:

Vcc	GND	Function
G12,C6	G11,B7	Internal Logic supply pins
L8	L6,L9	Address bus output buffer supply pins
G3	D3,J3	Data bus output buffer supply pins
C9	E11	Port B and C output buffer supply pins

Power and Ground Connections for PGA

Vcc	GND	Function
35, 36, 128, 129	33, 34, 130, 131	Internal Logic supply pins
63, 64	55, 56, 73, 74	Address bus output buffer supply pins
100, 101	90, 91, 111, 112	Data bus output buffer supply pins
12, 13	23, 24	Port B and C output buffer supply pins

Power and Ground Connections for CQFP and PQFP

Power and Ground Connections

The Vcc power supply should be bypassed to ground using at least four 0.1 uF by- pass capacitors located either underneath the chip or as close as possible to the four sides of the package. The capacitor leads and associated printed circuit traces connecting to chip Vcc and Gnd should be kept to less than 1/2" per capacitor lead. A four-layer board is recommended, employing two inner layers as Vcc and Gnd planes. All output pins on the DSP56001 have fast rise and fall times — typically less than 3 ns. with a 10 pf. load. Printed circuit (PC) trace interconnection length should be minimized in order to minimize undershoot and reflections caused by these fast output switching times. This recommendation particularly applies to the address and data buses as well as the $\overline{RD}$, $\overline{WR}$, $\overline{IRQA}$, $\overline{IRQB}$, and $\overline{HEN}$ pins. Maximum PC trace lengths on the order of 6" are recommended. Capacitance calculations should consider all device loads as well as parasitic capacitances due to the PC traces. Attention to proper PCB layout and bypassing becomes especially critical in systems with higher capacitive loads because these loads create higher transient currents in the Vcc and GND circuits. Pull up/down all unused inputs or signals that will be inputs during reset.

Signal Stability

When designing hardware to interface with the Host Interface, it is important to ensure that all signals be clean and free from noise. Particular attention should be given to the quality of the Host Enable ($\overline{HEN}$). All inputs to the port should be stable when $\overline{HEN}$ is asserted and should remain stable until $\overline{HEN}$ has fully returned to the deasserted state. It is important to note that such phenomena as ground-bounce and cross-talk can inadvertently cause $\overline{HEN}$ to temporarily rise above $V_{il\ max}$. Should this occur without completing the full logic transition to $V_{ih\ min}$, the DSP56001 Host Port may not correctly update the port status information which can result in storing two or more copies of a single down loaded data word. Of course, if a full logic transition occurs, the part will complete a normal data transfer operation.

DSP56001 Electrical Characteristics

DC Electrical Characteristics (Vcc = 5.0 Vdc ± 10%; T_J = -40 to +105° C at 20.5 MHz and 27 MHz)
(Vcc = 5.0 Vdc ± 5%; T_J = -40 to +105° C at 33 MHz)

Characteristic	Symbol	Min	Typ	Max	Unit
Supply Voltage 20, 27 MHz 33 MHz	Vcc	4.5 4.75	5.0	5.5 5.25	V
Input High Voltage Except EXTAL, $\overline{\text{RESET}}$, MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$	V_{IH}	2.0	—	Vcc	V
Input Low Voltage Except EXTAL, MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$	V_{IL}	-0.5	—	0.8	V
Input High Voltage EXTAL	V_{IHC}	4.0	—	Vcc	V
Input Low Voltage EXTAL	V_{ILC}	-0.5	—	0.6	V
Input High Voltage $\overline{\text{RESET}}$	V_{IHR}	2.5	—	Vcc	V
Input High Voltage MODA/$\overline{\text{IRQA}}$ and MODB/$\overline{\text{IRQB}}$	V_{IHM}	3.5	—	Vcc	V
Input Low Voltage MODA/$\overline{\text{IRQA}}$ and MODB/$\overline{\text{IRQB}}$	V_{ILM}	-0.5	—	2.0	V
Input Leakage Current EXTAL, $\overline{\text{RESET}}$, MODA/$\overline{\text{IRQA}}$, MODB/$\overline{\text{IRQB}}$, $\overline{\text{BR}}$	I_{in}	-1	—	1	uA
Three-State (Off-State) Input Current (@2.4 V/0.4 V)	I_{TSI}	-10	—	10	uA
Output High Voltage (I_{OH} = -0.4 mA)	V_{OH}	2.4	—	—	V
Output Low Voltage (I_{OL} = 1.6 mA; $\overline{\text{RD}}$, $\overline{\text{WR}}$ I_{OL} = 1.6 mA; Open Drain $\overline{\text{HREQ}}$ I_{OL} = 6.7 mA, TXD IOL = 6.7 mA)	V_{OL}	—	—	0.4	V
Total Supply Current 5.25 V, 33 MHz 5. 5 V, 27 MHz 5. 5 V, 20 MHz in WAIT Mode (see Note 1) in STOP Mode (see Note 1)	I_{DD33} I_{DD27} I_{DD20} I_{DDW} I_{DDS}	— — — — —	160 130 100 10 100	185 155 115 25 2000	mA mA mA mA µA
Input Capacitance (see Note 2)	Cin	—	10	—	pf

Notes:

1. In order to obtain these results all inputs must be terminated (i.e., not allowed to float).
2. Periodically sampled and not 100% tested.

DSP56001 Electrical Characteristics

AC Electrical Characteristics

The timing waveforms in the **AC Electrical Characteristics** are tested with a V_{IL} maximum of 0.5 V and a V_{IH} minimum of 2.4 V for all pins, except EXTAL, $\overline{\text{RESET}}$, MODA, and MODB. These four pins are tested using the input levels set forth in the **DC Electrical Characteristics**. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition. DSP56001 output levels are measured with the production test machine V_{OL} and V_{OH} reference levels set at 0.8 V and 2.0 V respectively.

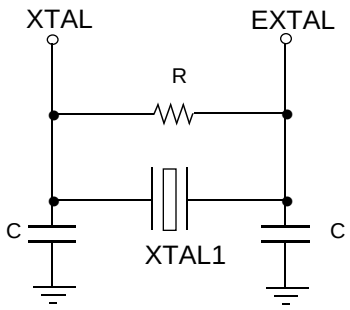
AC Electrical Characteristics - Clock Operation

The DSP56001 system clock may be derived from the on-chip crystal oscillator as shown in Clock Figure 1, or it may be externally supplied. An externally supplied square wave voltage source should be connected to EXTAL, leaving XTAL physically unconnected (see Clock Figure 2) to the board or socket. The rise and fall time of this external clock should be 5 ns maximum.

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
	Frequency of Operation (EXTAL Pin)	4.0	20.5	4.0	27.0	4.0	33.0	MHz

Notes:

1. External Clock Input High and External Clock Input Low are measured at 50% of the input transition. tch and tcl are dependent on the duty cycle.
2. T = Icyc / 4 is used in the electrical characteristics. T represents an average which is independent of the duty cycle.

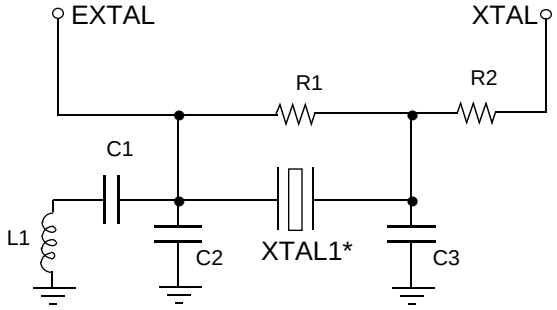


Fundamental Frequency Crystal Oscillator

Suggested Component Values
For f_{osc} = 4 MHz:
R = 680 KΩ ± 10%
C = 20 pf ± 20%

For f_{osc} = 30 MHz:
R = 680 KΩ ± 10%
C = 20 pf ± 20%

Notes:
(1) The suggested crystal source is ICM, # 433163 - 4.00 (4MHz fundamental, 20 pf load) or # 436163 - 30.00 (30 MHz fundamental, 20 pf load).

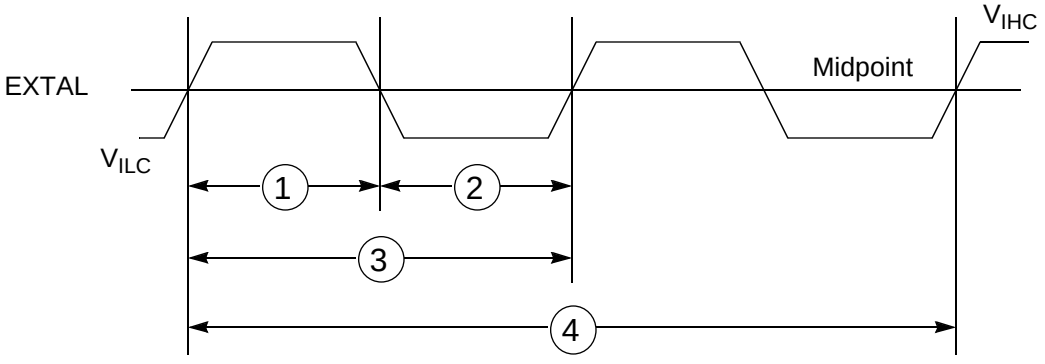


3rd Overtone Crystal Oscillator

Suggested Component Values
R1 = 470 KΩ ± 10%
R2 = 330 Ω ± 10%
C1 = 0.1 µf ± 20%
C2 = 26 pf ± 20%
C3 = 20 pf ± 10%
L1 = 2.37 µH ± 10%
XTAL =33 MHz, AT cut, 20 pf load,
50Ω max series resistance

Notes:
(1) *3rd overtone crystal.
(2) The suggested crystal source is ICM, # 471163 - 33.00 (33 MHz 3rd overtone, 20 pf load).
(3) R2 limits crystal current
(4) Reference Benjamin Parzen, The Design of Crystal and Other Harmonic Oscillators, John Wiley& Sons, 1983

Clock Figure 1. Crystal Oscillator Circuits



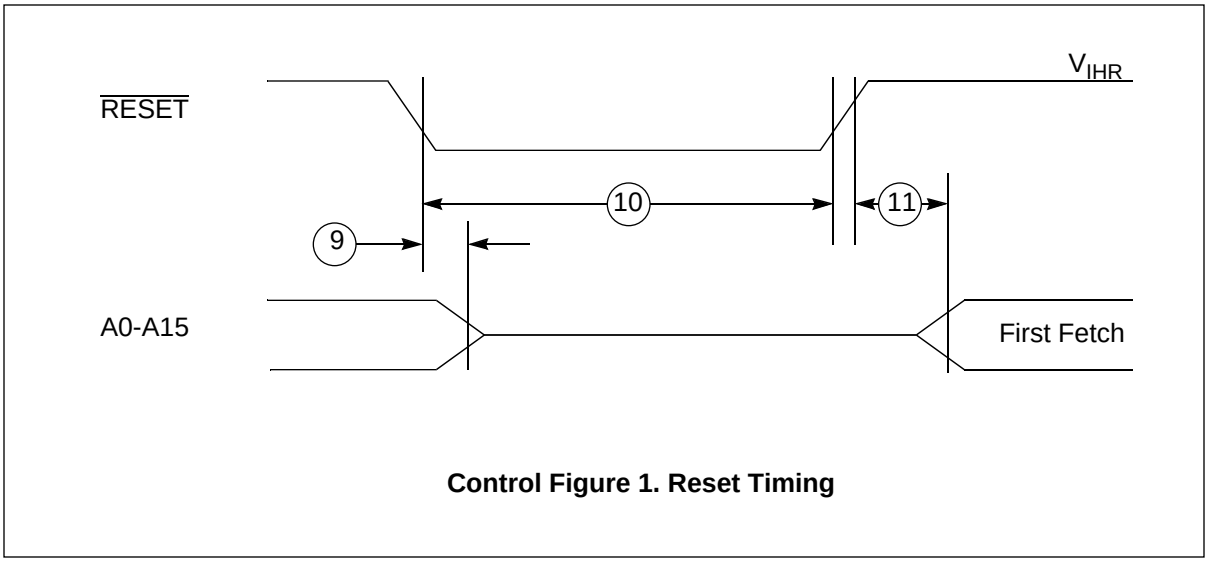
Note: The midpoint is V_{ILC} + 0.5 (V_{IHC} - V_{ILC}).

Clock Figure 2. External Clock Timing

AC Electrical Characteristics - Reset, Stop, Mode Select and Interrupt Timing

(Vcc = 5.0 Vdc ±10%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz)
(Vcc = 5.0 Vdc ± 5%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz)
(See Control Figure 1 through 8)
cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
WS = Number of wait states (1 WS = 1 cyc = 2T) programmed into external bus access using BCR (WS = 0 - 15)
tch = Clock high period
tcl = Clock low period

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
9	Delay from $\overline{\text{RESET}}$ Assertion to Address High Impedance (periodically sampled and not 100% tested)	—	50	—	38	—	31	ns
10	Minimum Stabilization Duration Internal Osc. (see Note 1) External Clock (see Note 2)	75000*cyc 25*cyc	— —	75000*cyc 25*cyc	— —	75000*cyc 25*cyc	— —	ns ns
11	Delay from Asynchronous $\overline{\text{RESET}}$ Deassertion to First External Address Output (Internal Reset Negation)	8*cyc	9*cyc+40	8*cyc	9*cyc+31	8*cyc	9*cyc+25	ns
12	Synchronous Reset Setup Time from $\overline{\text{RESET}}$ Deassertion to Falling Edge of External Clock	20	cyc-10	15	cyc-8	13	cyc-7	ns
13	Synchronous Reset Delay Time from the Synchronous Falling Edge of External Clock to the First External Address Output	8*cyc+5	8*cyc+30	8*cyc+5	8*cyc+23	8*cyc+5	8*cyc+19	ns
14	Mode Select Setup Time	100	—	77	—	62	—	ns
15	Mode Select Hold Time	0	—	0		0		ns
16 16a	Edge-Triggered Interrupt Request assertion deassertion	25 15	— —	17 10	— —	16 10	— —	ns ns



Control Figure 1. Reset Timing

NOTE

*When using fast interrupts and **$\overline{IRQA}$ and $\overline{IRQB}$** are defined as **level**-sensitive, then timings 19 through 22 apply to prevent multiple interrupt service. To avoid these timing restrictions, the negative edge-triggered mode is recommended when using fast interrupt. Long interrupts are recommended when using level-sensitive mode.*

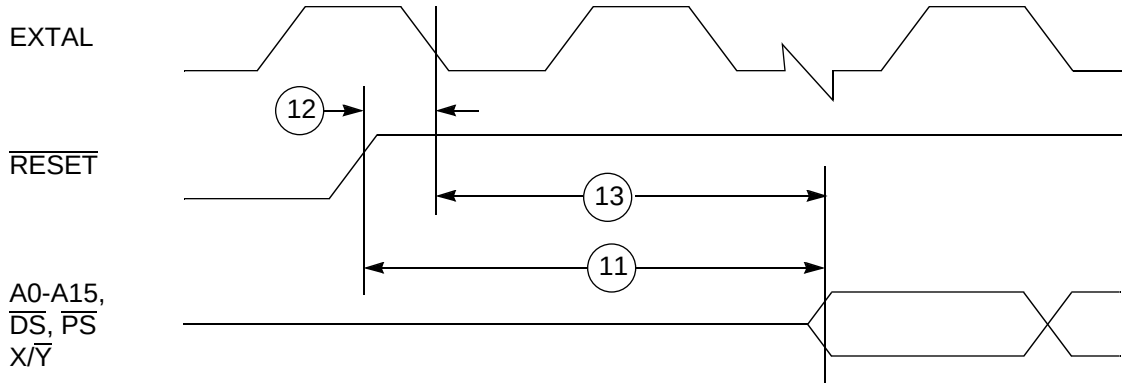
Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
17	Delay from $\overline{IRQA}$, $\overline{IRQB}$ Assertion to External Memory Access Address Out Valid Caused by First Interrupt Instruction Fetch Instruction Execution	 5*cyc+tch 9*cyc+tch	 — —	 5*cyc+tch 9*cyc+tch	 — —	 5*cyc+tch 9*cyc+tch	 — —	 ns ns
18	Delay from $\overline{IRQA}$, $\overline{IRQB}$ Assertion to General Purpose Transfer Output Valid Caused by First Interrupt Instruction Execution	11+cyc +tch	—	11*cyc +tch	—	11*cyc +tch	—	ns
19	Delay from Address Output Valid Caused by First Interrupt Instruction Execution to Interrupt Request Deassertion for Level Sensitive Fast Interrupts	—	2*cyc+tcl+ (cyc*WS) -44	—	2*cyc+tcl+ (cyc*WS) -34	—	2*cyc+tcl+ (cyc*WS) -27	ns
20	Delay from $\overline{RD}$ Assertion to Interrupt Request Deassertion for Level Sensitive Fast Interrupts	—	2*cyc+ (cyc*WS) -40	—	2*cyc+ (cyc*WS) -31	—	2*cyc+ (cyc*WS) -25	ns
21	Delay from $\overline{WR}$ Assertion to WS=0 Interrupt Request Deassertion for WS>0 Level Sensitive Fast Interrupts	— —	2*cyc-40 cyc+tcl+ (cyc*WS) -40	— —	2*cyc-31 cyc+tcl+ (cyc*WS) -31	— —	2*cyc-25 cyc+tcl+ (cyc*WS) -25	ns ns
22	Delay from General-Purpose Output Valid to Interrupt Request Deassertion for Level Sensitive Fast Interrupts - If Second Interrupt Instruction is: Single Cycle Two Cycle	 — —	 tcl-60 (2*cyc)+tcl -60	 — —	 tcl-46 (2*cyc)+tcl -46	 — —	 tcl-37 (2*cyc)+tcl -37	 ns ns

AC Electrical Characteristics - Reset, Stop, Mode Select, and Interrupt Timing (Continued)

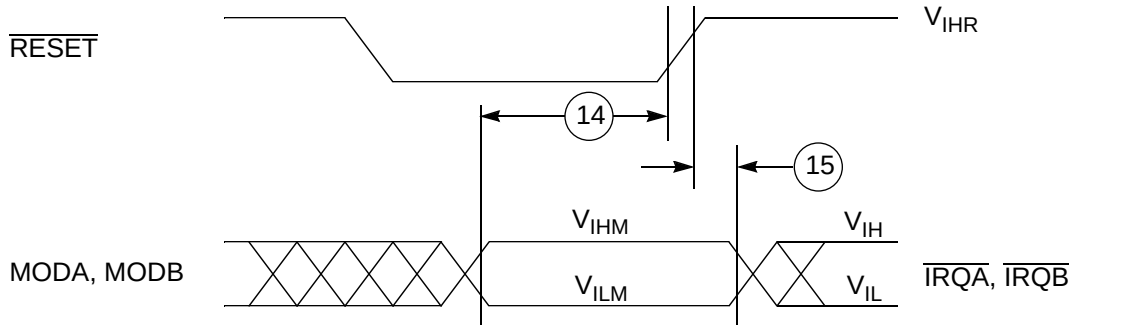
Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
23	Synchronous Interrupt Setup Time from $\overline{\text{IRQA}}$, $\overline{\text{IRQB}}$ Assertion to the Synchronous Rising Edge of External Clock (see Notes 5, 6)	25	cyc-10	19	cyc-8	16	cyc-7	ns
24	Synchronous Interrupt Delay Time from the Synchronous Rising Edge of External Clock to the First External Address Output Valid Caused by the First Instruction Fetch after Coming out of Wait State (see Notes 3, 5)	13*cyc+ tch+8	13*cyc+ tch+30	13*cyc+ tch+6	13*cyc+ tch+23	13*cyc+ tch+5	13*cyc+ tch+19	ns
25	Duration for $\overline{\text{IRQA}}$ Assertion to Recover from Stop State (see Note 4)	25	—	19	—	16	—	ns
26	Delay from $\overline{\text{IRQA}}$ Assertion to Fetch of First Instruction (for Stop) for Internal Osc / OMR bit 6 = 0 External Clock / OMR bit 6 = 1 (see Notes 1, 2, and 7)	 65545*cyc 17*cyc	 — —	 65545*cyc 17*cyc	 — —	 65545*cyc 17*cyc	 — —	 ns ns
27	Duration for Level Sensitive $\overline{\text{IRQA}}$ Assertion to Fetch of First Interrupt Instruction (for Stop) for Internal Osc / OMR bit 6 = 0 External Clock / OMR bit 6 = 1 (see Notes 1, 2, and 7)	 65533*cyc +tcl 5*cyc+tcl	 — —	 65533*cyc +tcl 5*cyc+tcl	 — —	 65533*cyc +tcl 5*cyc+tcl	 — —	 ns ns
28	Delay from Level Sensitive $\overline{\text{IRQA}}$ Assertion to Fetch of First Interrupt Instruction (for Stop) for Internal Osc / OMR bit 6 = 0 External Clock / OMR bit 6 = 1 (see Notes 1, 2, and 7)	 65545*cyc 17*cyc	 — —	 65545*cyc 17*cyc	 — —	 65545*cyc 17*cyc	 — —	 ns ns

Notes:

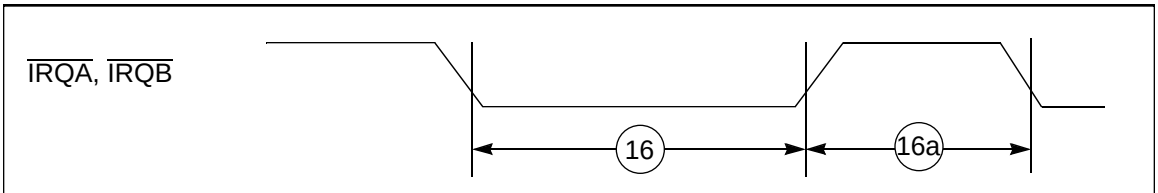
1. A clock stabilization delay is required when using the on-chip crystal oscillator in two cases:
   1) after power-on reset, and
   2) when recovering from Stop mode.
   During this stabilization period, T will not be constant. Since this stabilization period varies, a delay of 150,000T is typically allowed to assure that the oscillator is stabilized before executing programs. While it is possible to set OMR bit 6 = 1 when using the internal crystal oscillator, it is not recommended and these specifications do not guarantee timings for that case. See Section 8.5 in the *DSP56000/DSP56001 User's Manual* for additional information.
2. Circuit stabilization delay is required during reset when using an external clock in two cases:
   1) after power-on reset, and
   2) when recovering from Stop mode.
3. For Revision B silicon, the min and max numbers are 12cyc+Tch+8 and 12cyc+Tch+30, respectively.
4. The minimum is specified for the duration of an edge triggered $\overline{\text{IRQA}}$ interrupt required to recover from the STOP state without having the $\overline{\text{IRQA}}$ interrupt accepted.
5. Timing #23 is for all IRQx interrupts while timing #24 is only when exiting WAIT.
6. Timing #23 triggers off T1 in the normal state and off T1/T3 when exiting the WAIT state.
7. The timings in the table are for Rev. C parts. The timings for Rev. C parts are shorter by 1 cyc than the Rev. B parts when OMR6=0.



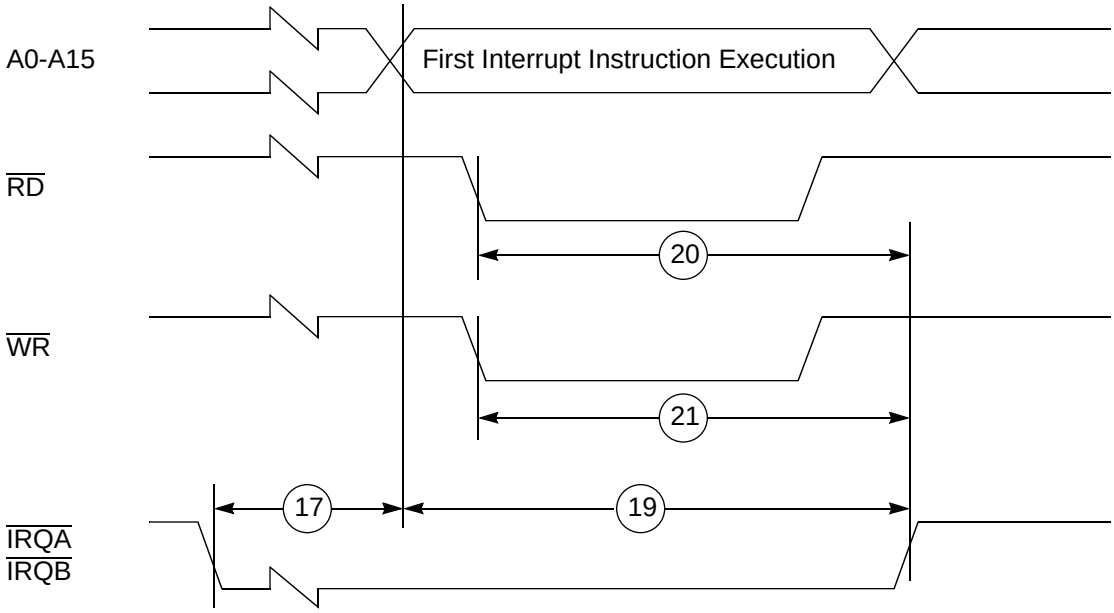
Control Figure 2. Synchronous Reset Timing



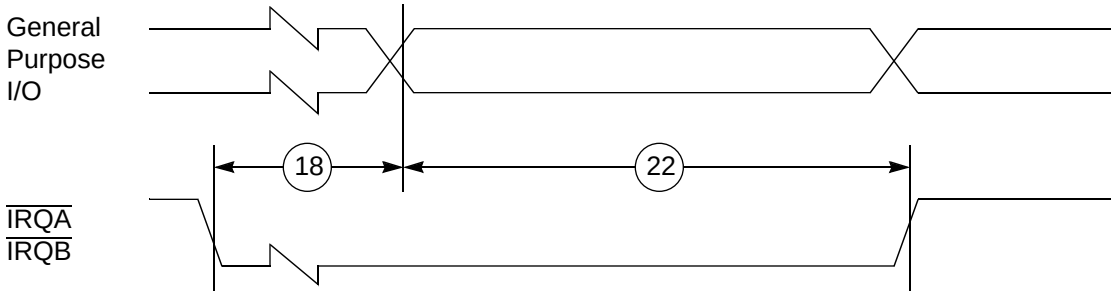
Control Figure 3. Operating Mode Select Timing



Control Figure 4. External Interrupt Timing (Negative Edge-Triggered)

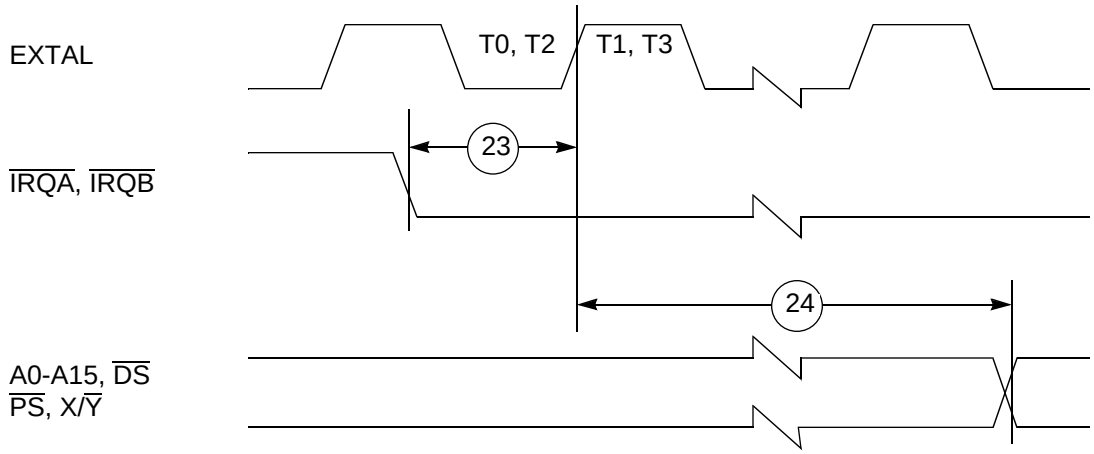


a) First Interrupt Instruction Execution

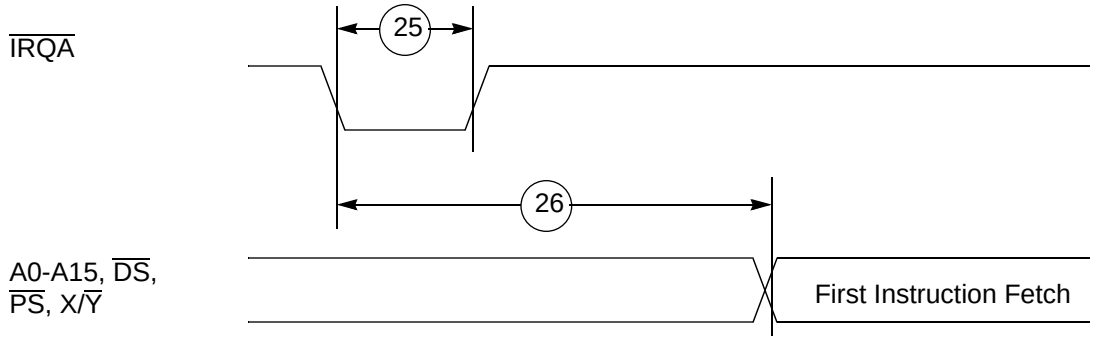


b) General Purpose I/O

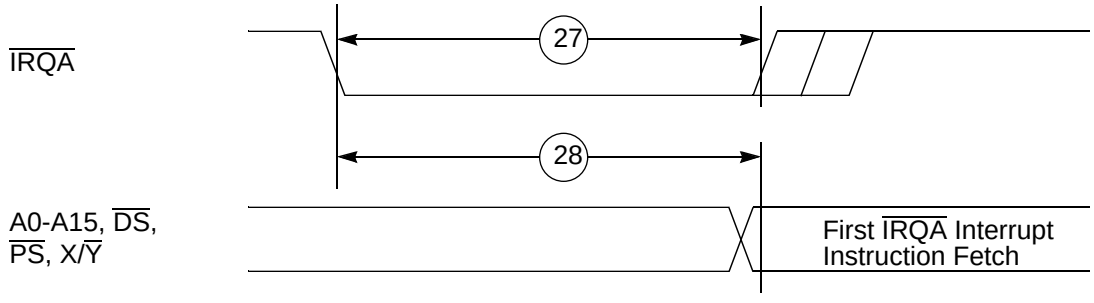
Control Figure 5. External Level-Sensitive Fast Interrupt Timing



Control Figure 6. Synchronous Interrupt and Synchronous Wait State Timing



Control Figure 7. Recovery from Stop State Using IRQA



Control Figure 8. Recovery from Stop State Using IRQA Interrupt Service

HOST PORT USAGE CONSIDERATIONS

Careful synchronization is required when reading multibit registers that are written by another asynchronous system. This is a common problem when two asynchronous systems are connected. The situation exists in the Host port. The considerations for proper operation are discussed below.

Host Programmer Considerations

1. Unsynchronized Reading of Receive Byte Registers
   When reading receive byte registers, RXH, RXM, or RXL, the Host programmer should use interrupts or poll the RXDF flag which indicates that data is available. This assures that the data in the receive byte registers will be stable.

2. Overwriting Transmit Byte Registers
   The Host programmer should not write to the transmit byte registers, TXH, TXM, or TXL, unless the TXDE bit is set indicating that the transmit byte registers are empty. This guarantees that the transmit byte registers will transfer valid data to the HRX register.

3. Synchronization of Status Bits from DSP to Host
   HC, HREQ, DMA, HF3, HF2, TRDY, TXDE, and RXDF (refer to *DSP56000/DSP56001 User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions of these status bits) status bits are set or cleared from inside the DSP and read by the Host processor. The Host can read these status bits very quickly without regard to the clock rate used by the DSP, but the possibility exists that the state of the bit could be changing during the read operation. This is generally not a system problem, since the bit will be read correctly in the next pass of any Host polling routine.

   However, if the Host asserts the $\overline{\text{HEN}}$ for more than timing number 31a (T31a), with a minimum cycle time of timing number 32a (T32a), then the status is guaranteed to be stable.

   A potential problem exists when reading status bits HF3 and HF2 as an encoded pair. If the DSP changes HF3 and HF2 from 00 to 11, there is a small probability that the Host could read the bits during the transition and receive 01 or 10 instead of 11. If the combination of HF3 and HF2 has significance, the Host could read the wrong combination.

   Solution:
   a. Read the bits twice and check for consensus.
   b. Assert $\overline{\text{HEN}}$ access for T31a so that status bit transitions are stabilized.

4. Overwriting the Host Vector
   The Host programmer should change the Host Vector register only when the Host Command bit (HC) is clear. This change will guarantee that the DSP interrupt control logic will receive a stable vector.

5. Cancelling a Pending Host Command Exception
   The Host processor may elect to clear the HC bit to cancel the Host Command Exception request at any time before it is recognized by the DSP. Because the Host does not know exactly when the exception will be recognized (due to exception processing synchronization and pipeline delays), the DSP may execute the Host exception after the HC bit is cleared. For these reasons, the HV bits must not be changed at the same time the HC bit is cleared.

DSP Programmer Considerations

1. Reading HF0 and HF1 as an Encoded Pair
   DMA, HF1, HF0, and HCP, HTDE, and HRDF (refer to *DSP56000/DSP56001 User's Manual*, I/O Interface section, Host/DMA Interface Programming Model for descriptions of these status bits) status bits are set or cleared by the Host processor side of the interface. These bits are individually synchronized to the DSP clock.

   A potential problem exists when reading status bits HF1 and HF2 as an encoded pair, i.e., the four combinations 00, 01, 10, and 11 each have significance. A very small probability exists that the DSP will read the status bits synchronized during transition. The solution to this potential problem is to read the bits twice for consensus.

DSP56001 Electrical Characteristics

AC Electrical Characteristics - Host I/O Timing

(Vcc = 5.0 Vdc ± 10%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz)
(Vcc = 5.0 Vdc ± 5%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz)
(see Host Figures 1 through 6)
cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
tHSDL = Host Synchronization Delay Time
Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
30	Host Synchronous Delay (see Note 1)	tcl	cyc+tcl	tcl	cyc+tcl	tcl	cyc+tcl	ns
31	$\overline{HEN}/\overline{HACK}$ Assertion Width (see Note 2) a.CVR, ICR, ISR Read (see Note 4) b.Read c.Write	 cyc+60 50 25	 — — —	 cyc+46 39 19	 — — —	 cyc+37 31 16	 — — —	 ns ns ns
32	$\overline{HEN}/\overline{HACK}$ Deassertion Width (see Note 2 and 5)	25	—	19	—	16	—	ns
32a	Minimum Cycle Time Between Two $\overline{HEN}$ Assertion for Consecutive CVR, ICR, and ISR Reads (see Note 2)	2*cyc+60	—	2*cyc+46	—	2*cyc+37	—	ns
33	Host Data Input Setup Time Before $\overline{HEN}/\overline{HACK}$ Deassertion	5	—	4	—	4	—	ns
34	Host Data Input Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	5	—	4	—	4	—	ns
35	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Active from High Impedance	0	—	0	—	0	—	ns
36	$\overline{HEN}/\overline{HACK}$ Assertion to Output Data Valid (periodically sampled, and not 100% tested)	—	50	—	39	—	31	ns
37	$\overline{HEN}/\overline{HACK}$ Deassertion to Output Data High Impedance	—	35	—	27	—	22	ns
38	Output Data Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	5	—	4	—	4	—	ns
39	HR/$\overline{W}$ Low Setup Time Before $\overline{HEN}$ Assertion	0	—	0	—	0	—	ns
40	HR/$\overline{W}$ Low Hold Time After $\overline{HEN}$ Deassertion	5	—	4	—	4	—	ns
41	HR/$\overline{W}$ High Setup Time to $\overline{HEN}$ Assertion	0	—	0	—	0	—	ns
42	HR/$\overline{W}$ High Hold Time After $\overline{HEN}/\overline{HACK}$ Deassertion	5	—	4	—	4	—	ns
43	HA0-HA2 Setup Time Before $\overline{HEN}$ Assertion	0	—	0	—	0	—	ns
44	HA0-HA2 Hold Time After $\overline{HEN}$ Deassertion	5	—	4	—	4	—	ns
45	DMA $\overline{HACK}$ Assertion to $\overline{HREQ}$ Deassertion (see Note 3)	5	60	4	46	4	49	ns

DSP56001 Electrical Characteristics

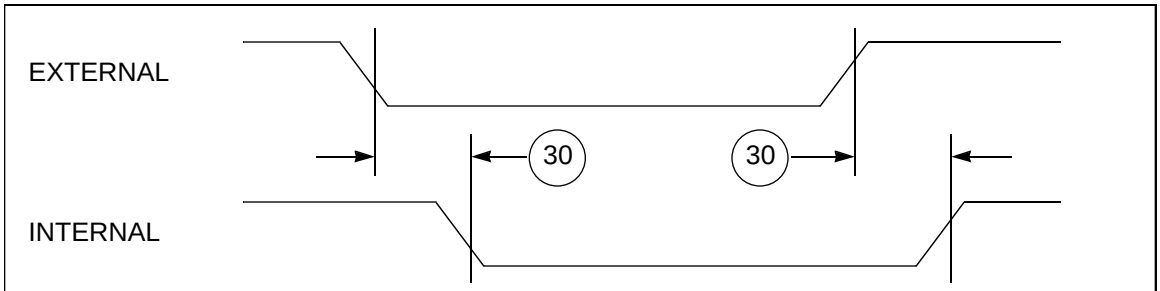
AC Electrical Characteristics - Host I/O Timing (Continued)

(Vcc = 5.0 Vdc ± 10%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz
(Vcc = 5.0 Vdc ± 5%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz,
see Host Figures 1 through 6)
cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
tHSDL = Host Synchronization Delay Time
Active low lines should be "pulled up" in a manner consistent with the AC and DC specifications

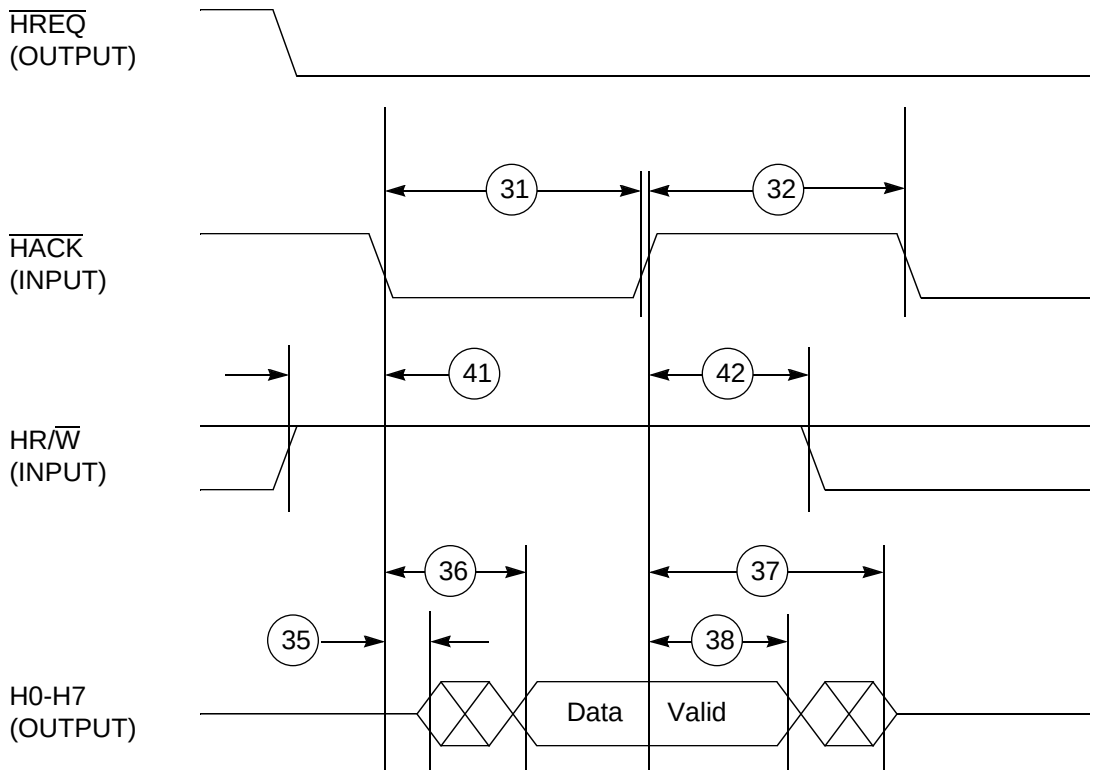
Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
46	DMA $\overline{\text{HACK}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion (see Note 3) for DMA RXL Read for DMA TXL Write for All Other Cases	 tHSDL+cyc +tch+5 tHSDL+cyc+5 5	 — — —	 tHSDL+cyc +tch+4 tHSDL+cyc+4 4	 — — —	 tHSDL+cyc +tch+4 tHSDL+cyc+4 4	 — — —	 ns ns ns
47	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for RXL Read (see Note 3)	tHSDL+cyc +tch+5	—	tHSDL+cyc +tch+4	—	tHSDL+cyc +tch+4	—	ns
48	Delay from $\overline{\text{HEN}}$ Deassertion to $\overline{\text{HREQ}}$ Assertion for TXL Write (see Note 3)	tHSDL+cyc+5	—	tHSDL+cyc+4	—	tHSDL+cyc+4	—	ns
49	Delay from $\overline{\text{HEN}}$ Assertion to $\overline{\text{HREQ}}$ Deassertion for RXL Read, TXL Write (see Note 3)	5	75	4	70	4	65	ns

Notes:

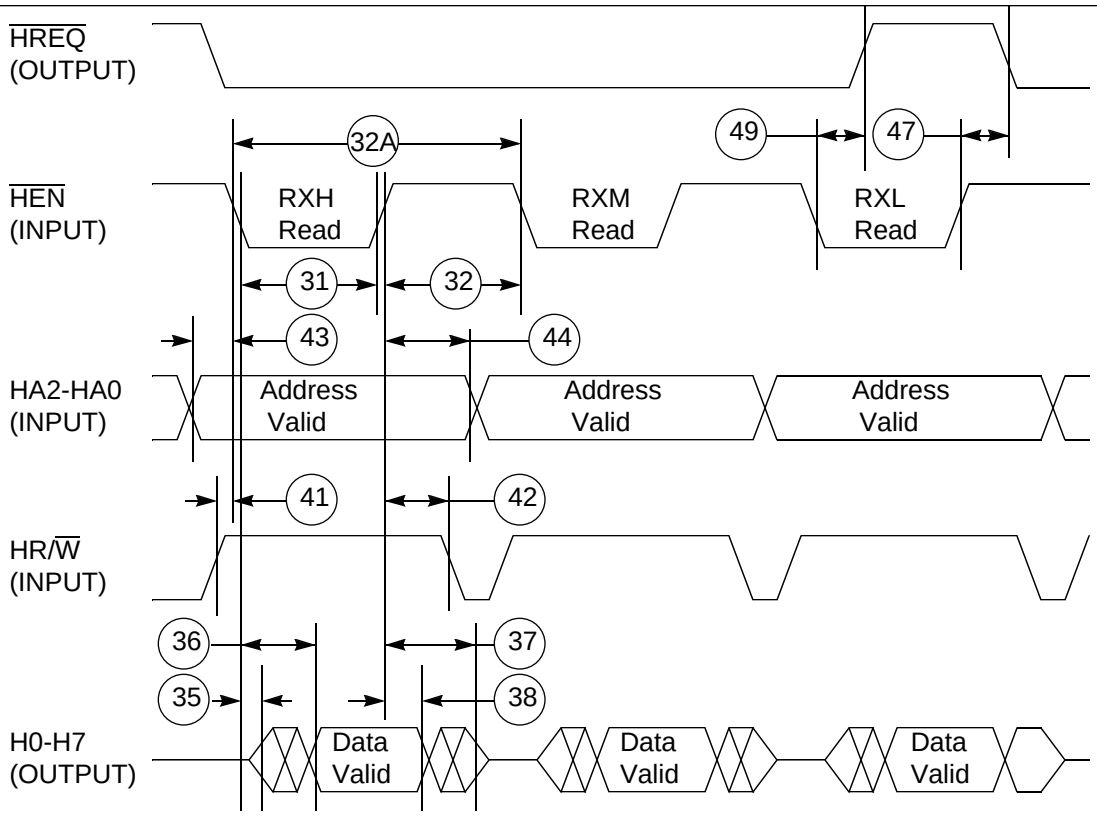
1. "Host synchronization delay (tHSDL)" is the time period required for the DSP56001 to sample any external asynchronous input signal, determine whether it is high or low, and synchronize it to the DSP56001 internal clock.
2. See **HOST PORT USAGE CONSIDERATIONS**.
3. $\overline{\text{HREQ}}$ is pulled up by a 1kΩ resistor.
4. This timing must be adhered to only if two consecutive reads from one of these registers are executed.
5. It is recommended that timing #32 be 2cyc+tch+10 minimum for 20.5 MHz, 2cyc+tch+7 minimum for 27 MHz, and 2cyc+tch+6 minimum for 33 MHz if two consecutive writes to TXL are executed without polling TXDE or $\overline{\text{HREQ}}$.



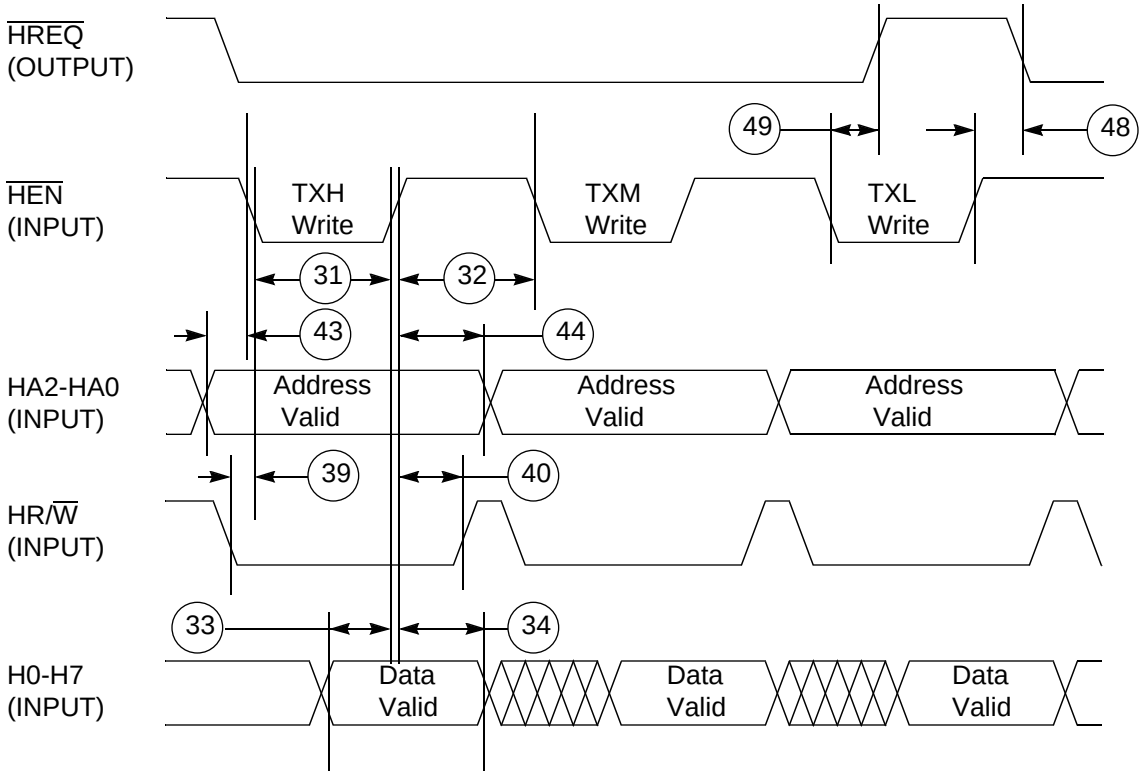
Host Figure 1. Host Synchronization Delay



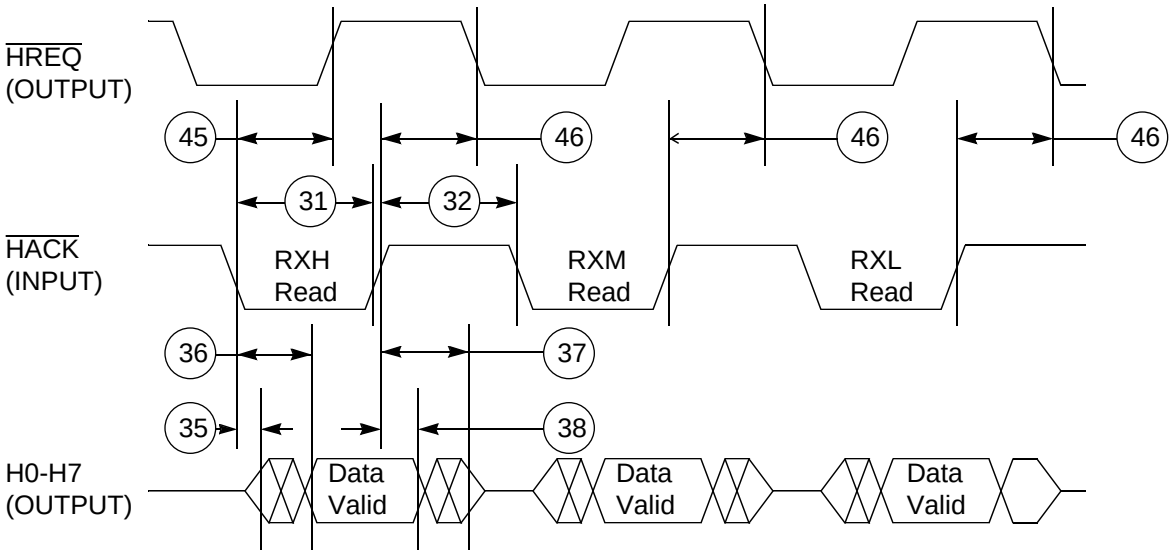
Host Figure 2. Host Interrupt Vector Register (IVR) Read



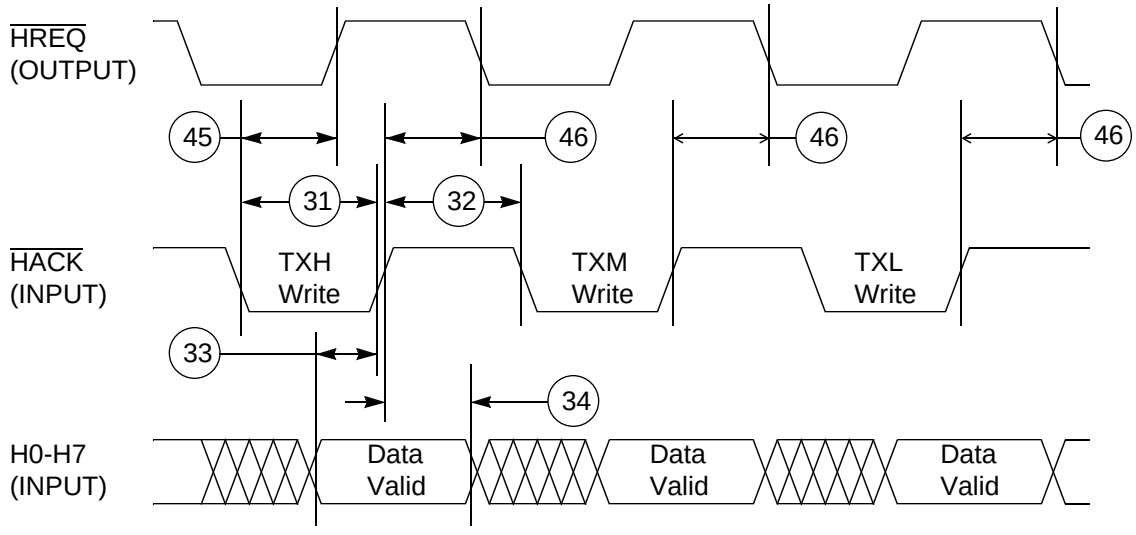
Host Figure 3. Host Read Cycle (Non-DMA Mode)



Host Figure 4. Host Write Cycle (Non-DMA Mode)



Host Figure 5. Host DMA Read Cycle



Host Figure 6. Host DMA Write Cycle

DSP56001 Electrical Characteristics

AC Electrical Characteristics - SCI Timing

(Vcc = 5.0 Vdc ± 10%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz,
Vcc = 5.0 Vdc ± 5%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz,
see SCI Figures 1 and 2)
cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
tSCC = Synchronous Clock Cycle Time (for internal clock tSCC is determined by the SCI clock control register and Icyc.)

SCI Synchronous Mode Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
55	Synchronous Clock Cycle — tSCC	8*cyc	—	8*cyc	—	8*cyc	—	ns
56	Clock Low Period	4*cyc-20	—	4*cyc-15	—	4*cyc-13	—	ns
57	Clock High Period	4*cyc-20	—	4*cyc-15	—	4*cyc-13	—	ns
59	Output Data Setup to Clock Falling Edge (Internal Clock)	2*cyc +tcl-50	—	2*cyc +tcl-39	—	2*cyc +tcl-31	—	ns
60	Output Data Hold After Clock Rising Edge (Internal Clock)	2*cyc -tcl-15	—	2*cyc -tcl-11	—	2*cyc -tcl-9	—	ns
61	Input Data Setup Time Before Clock Rising Edge (Internal Clock)	2*cyc +tcl+45	—	2*cyc +tcl+35	—	2*cyc +tcl+28	—	ns
62	Input Data Not Valid Before Clock Rising Edge (Internal Clock)	—	2*cyc +tcl-10	—	2*cyc +tcl-8	—	2*cyc +tcl-6	ns
63	Clock Falling Edge to Output Data Valid (External Clock)	—	63	—	48	—	39	ns
64	Output Data Hold After Clock Rising Edge (External Clock)	cyc+12	—	cyc+9	—	cyc+8	—	ns
65	Input Data Setup Time Before Clock Rising Edge (External Clock)	30	—	23	—	19	—	ns
66	Input Data Hold Time After Clock Rising Edge (External Clock)	40	—	31	—	25	—	ns

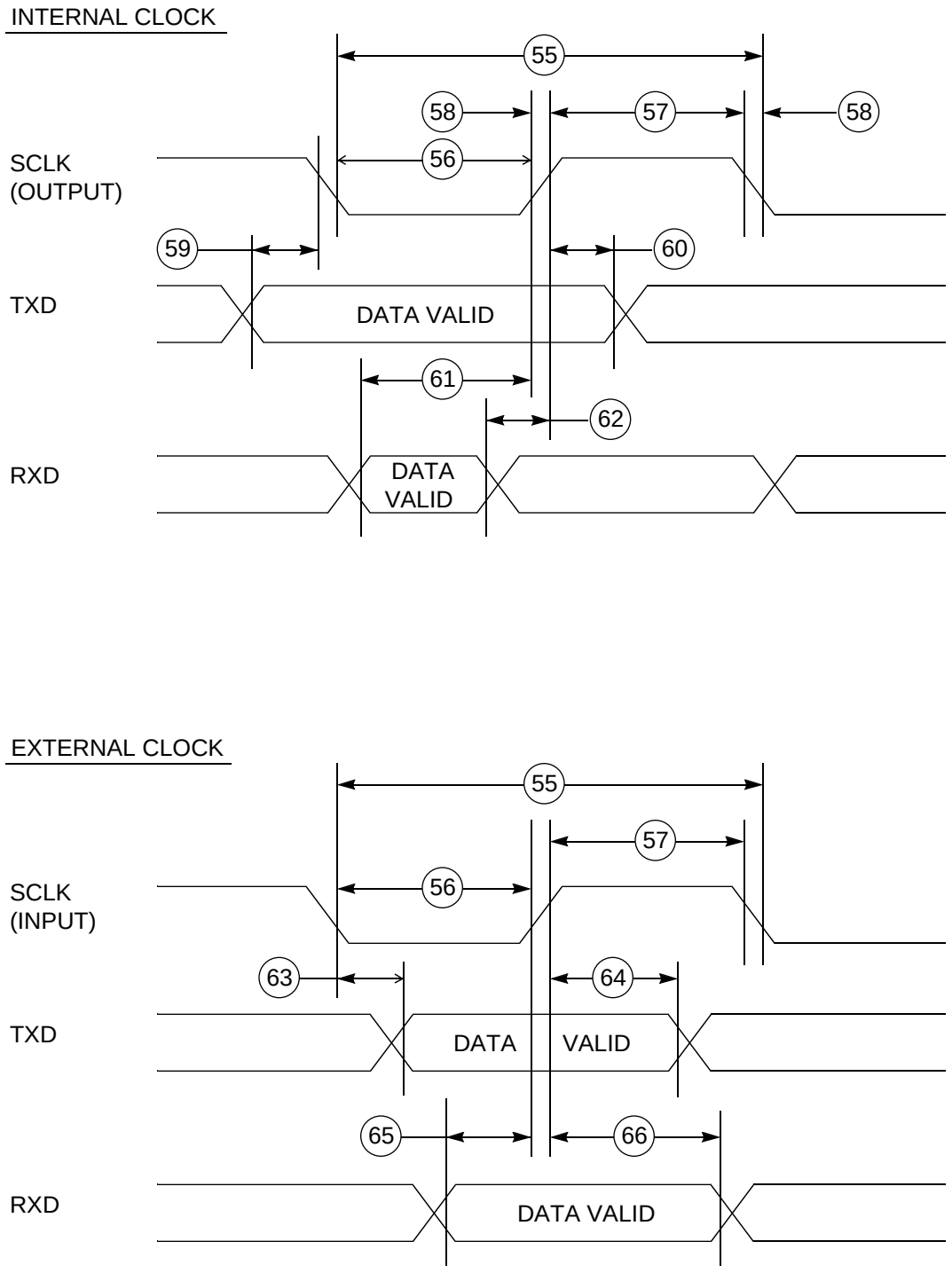
DSP56001 Electrical Characteristics

AC Electrical Characteristics - SCI Timing

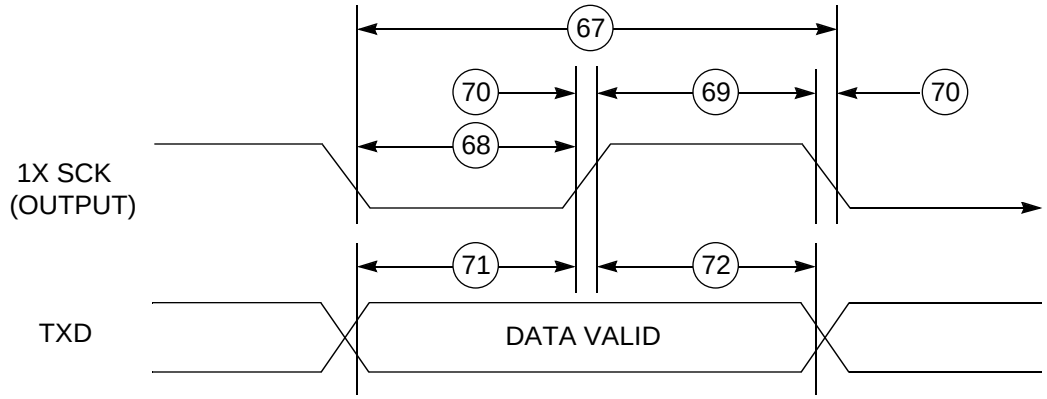
(Vcc = 5.0 Vdc ± 10%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz,
Vcc = 5.0 Vdc ± 5%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz,
see SCI Figures 1 and 2)
cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
tACC = Asynchronous clock cycle time
tACC = Asynchronous Clock Cycle Time (for internal clock tACC is determined by the SCI clock control register and Icyc)

SCI Asynchronous Mode Timing - 1X Clock

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
67	Asynchronous Clock Cycle	64*cyc	—	64*cyc	—	64*cyc	—	ns
68	Clock Low Period	32*cyc-20	—	32*cyc-15	—	32*cyc-13	—	ns
69	Clock High Period	32*cyc-20	—	32*cyc-15	—	32*cyc-13	—	ns
71	Output Data Setup to Clock Rising Edge (Internal Clock)	32*cyc -100	—	32*cyc -77	—	32*cyc -61	—	ns
72	Output Data Hold After Clock Rising Edge (Internal Clock)	32*cyc -100	—	32*cyc -77	—	32*cyc -61	—	ns



SCI Figure 1. SCI Synchronous Mode Timing



Note: In the wire-OR mode, TXD can be pulled up by 1KΩ

SCI Figure 2. SCI Asynchronous Mode Timing

DSP56001 Electrical Characteristics

AC Electrical Characteristics - SSI Timing

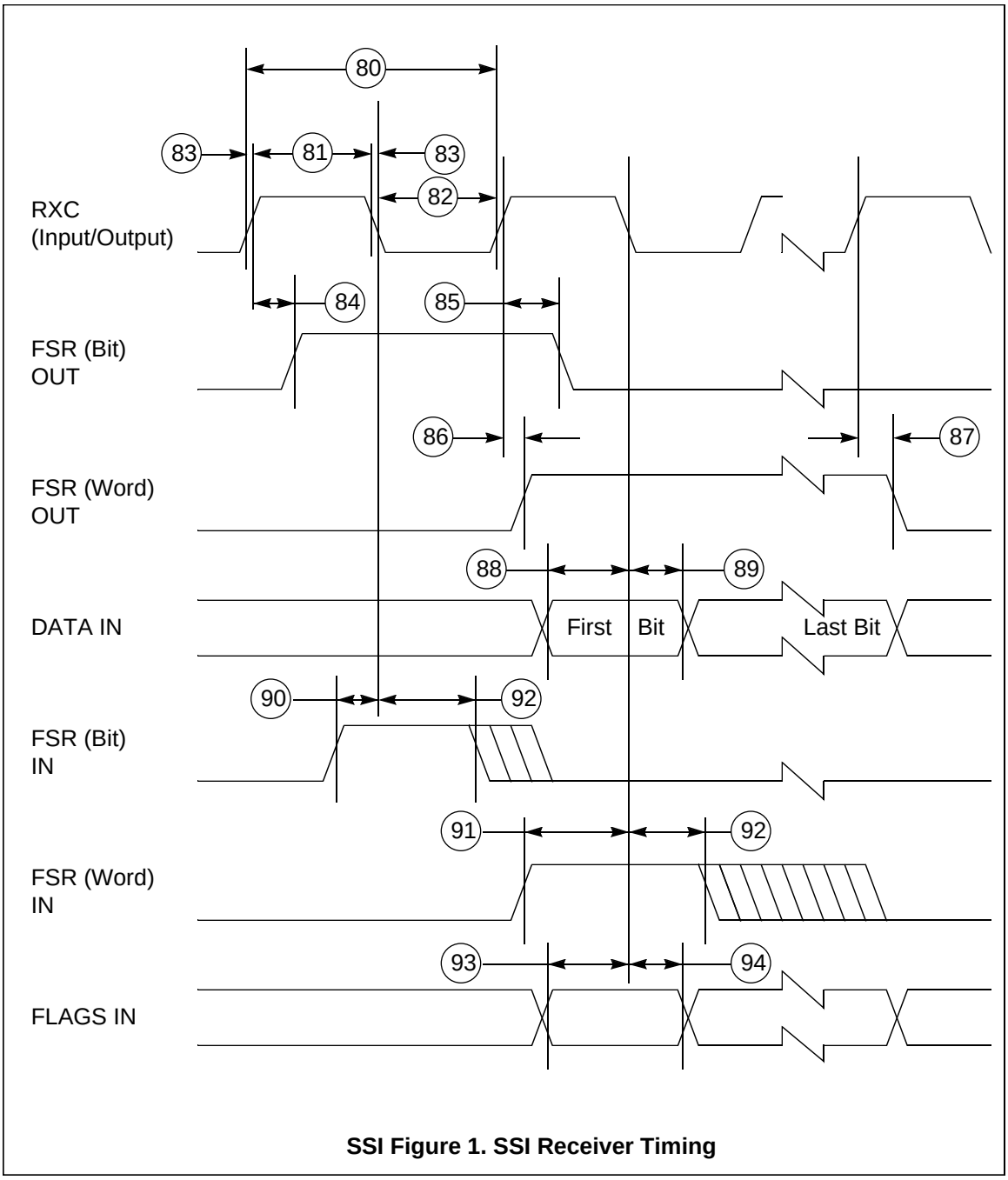
(Vcc = 5.0 Vdc ± 10%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz,
Vcc = 5.0 Vdc ± 5%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz,
see SSI Figures 1 and 2)
cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
tSSICC = SSI clock cycle time
TXC (SCK Pin) = Transmit Clock
RXC (SC0 or SCK Pin) = Receive Clock
FST (SC2 Pin) = Transmit Frame Sync
FSR (SC1 or SC2 Pin) = Receive Frame Sync
i ck = Internal Clock
x ck = External Clock
g ck = Gated Clock
i ck a = Internal Clock, Asynchronous Mode (Asynchronous implies that TXC and RXC are two different clocks)
i ck s = Internal Clock, Synchronous Mode (Synchronous implies that TXC and RXC are the same clock)
bl = bit length
wl = word length

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
80	Clock Cycle (see Note 1)	4*cyc	—	4*cyc	—	4*cyc	—	ns
81	Clock High Period	2*cyc-20	—	2*cyc-15	—	2*cyc-13	—	ns
82	Clock High Period	2*cyc-20	—	2*cyc-15	—	2*cyc-13	—	ns
84	RXC Rising Edge to FSR Out (bl) High							
	x ck	—	80	—	61	—	48	ns
	i ck a	—	50	—	38	—	31	ns
85	RXC Rising Edge to FSR Out (bl) Low							
	x ck	—	70	—	54	—	43	ns
	i ck a	—	40	—	31	—	25	ns
86	RXC Rising Edge to FSR Out (wl) High							
	x ck	—	70	—	54	—	43	ns
	i ck a	—	40	—	31	—	25	ns
87	RXC Rising Edge to FSR Out (wl) Low							
	x ck	—	70	—	54	—	43	ns
	i ck a	—	40	—	31	—	25	ns
88	Data In Setup Time Before RXC (SCK in Synchronous Mode) Falling Edge							
	x ck	15	—	12	—	10	—	ns
	i ck a	35	—	27	—	22	—	ns
	i ck s	25	—	19	—	16	—	ns
89	Data In Hold Time After RXC Falling Edge x ck	35	—	27	—	22	—	ns
	i ck a	5	—	4	—	4	—	ns
90	FSR Input (bl) High Before RXC Falling Edge x ck	15	—	12	—	10	—	ns
	i ck a	35	—	27	—	23	—	ns

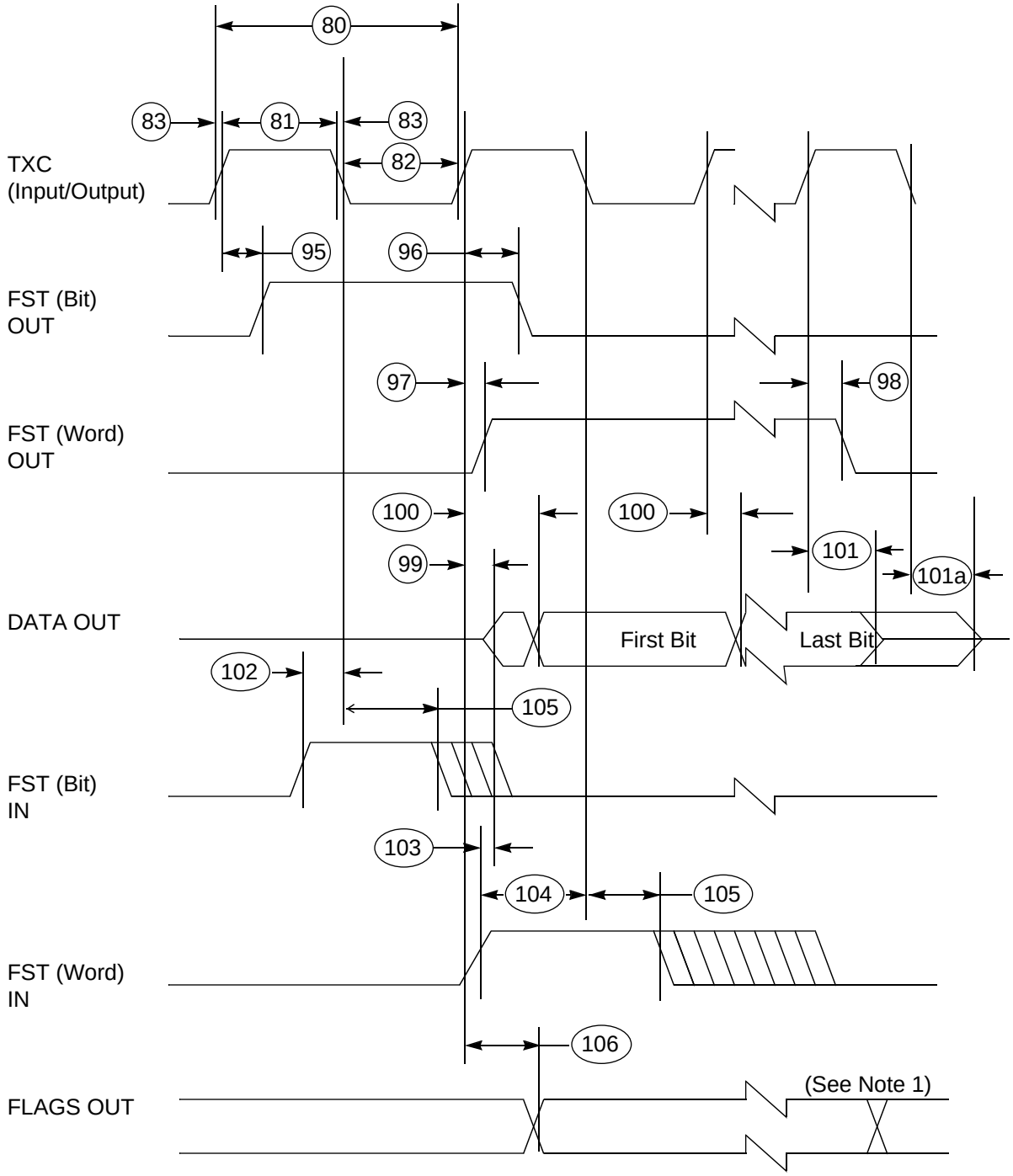
Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
93	Flags Input Setup Before RXC Falling Edge x ck i ck a	 30 50	 — —	 23 39	 — —	 19 31	 — —	 ns nss
94	Flags Input Hold Time After RXC Falling Edge x ck i ck a	 35 5	 — —	 27 4	 — —	 22 4	 — —	 ns ns
95	TXC Rising Edge to FST Out (bl) High x ck i ck a	 — —	 70 30	 — —	 54 23	 — —	 43 19	 ns ns
96	TXC Rising Edge to FST Out (bl) Low x ck i ck a	 — —	 65 35	 — —	 50 27	 — —	 40 22	 ns ns
97	TXC Rising Edge to FST Out (wl) High x ck i ck a	 — —	 65 35	 — —	 50 27	 — —	 40 22	 ns ns
98	TXC Rising Edge to FST Out (wl) Low x ck i ck a	 — —	 65 35	 — —	 50 27	 — —	 40 22	 ns ns
99	TXC Rising Edge to Data Out Enable from High Impedance x ck i ck a	 — —	 65 40	 — —	 50 31	 — —	 40 25	 ns ns
100	TXC Rising Edge to Data Out Valid x ck i ck a	 — —	 65 40	 — —	 50 31	 — —	 40 25	 ns ns
101	TXC Rising Edge to Data Out High Impedance (periodically sampled, and not 100% tested) x ck i ck a	 — —	 70 40	 — —	 54 31	 — —	 43 25	 ns ns
101a	TXC Falling Edge to Data Out High Impedance for Gated Clock Mode Only g ck	 cyc+tch	 —	 cyc+tch	 —	 cyc+tch	 —	 ns
102	FST Input (bl) Setup Time Before TXC Falling Edge x ck i ck a	 15 35	 — —	 12 27	 — —	 10 23	 — —	 ns ns
103	FST Input (wl) to Data Out Enable from High Impedance	—	60	—	46	—	37	ns
104	FST Input (wl) Setup Time Before TXC Falling Edge x ck i ck a	 20 55	 — —	 15 42	 — —	 13 34	 — —	 ns ns
105	FST Input Hold Time After TXC Falling Edge x ck i ck a	 35 5	 — —	 27 4	 — —	 22 4	 — —	 ns ns
106	Flag Output Valid After TXC Rising Edge x ck i ck a	 — —	 70 40	 — —	 54 31	 — —	 43 25	 ns ns

Note:

1. For internal clock, External Clock Cycle is defined by Icyc and SSI control register.



SSI Figure 1. SSI Receiver Timing



Note:

1. In the Network mode, output flag transitions can occur at the start of each time slot within the frame. In the Normal mode, the output flag state is asserted for the entire frame period.

SSI Figure 2. SSI Transmitter Timing

DSP56001 Electrical Characteristics

AC Electrical Characteristics — Capacitance Derating — External Bus Asynchronous Timing

Vcc = 5.0 Vdc ± 10%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 20.5 MHz and 27 MHz,

Vcc = 5.0 Vdc ± 5%, T_J = -40 to +105° C, CL = 50 pf + 1 TTL Load at 33 MHz, see Bus Figures 1 and 2

cyc = Clock cycle = 1/2 instruction cycle = 2 T cycles
WS = Number of Wait States, Determined by BCR Register (WS = 0 to 15)

The DSP56001 External Bus Timing Specifications are designed and tested at the maximum capacitive load of 50 pf, including stray capacitance. Typically, the drive capability of the External Bus pins (A0-A15, D0-D23, $\overline{PS}$, $\overline{DS}$, $\overline{RD}$, $\overline{WR}$, X/$\overline{Y}$) derates linearly at 1 ns per 12 pf of additional capacitance from 50 pf to 250 pf of loading. Port B and C pins derate linearly at 1 ns per 5 pf of additional capacitance from 50 pf to 250 pf of loading.

Active low inputs should be “pulled up” in a manner consistent with the AC and DC specifications.

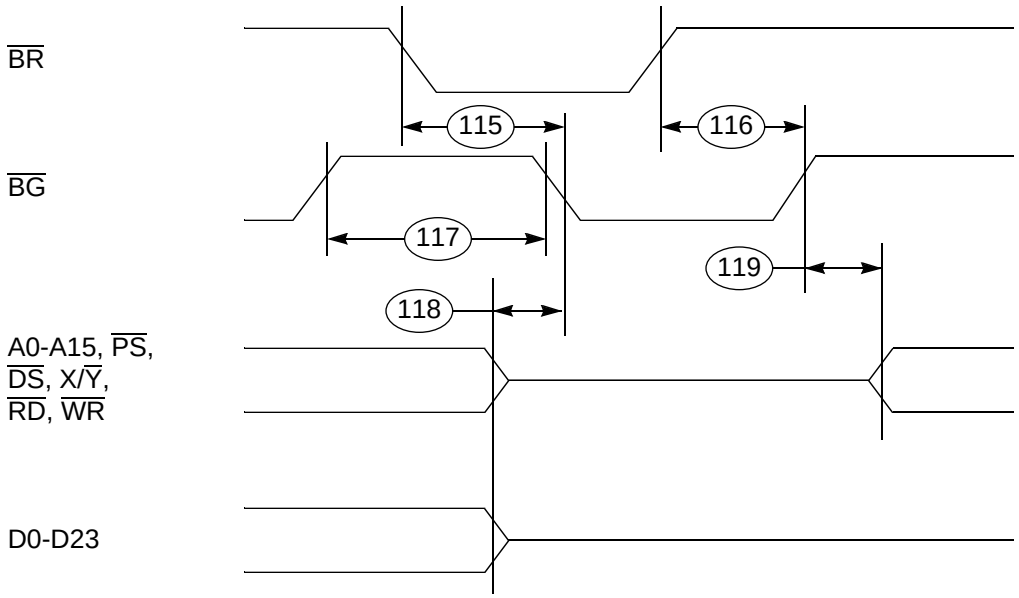
To conserve power, when an internal memory access follows an external memory access, the $\overline{RD}$ and $\overline{WR}$ strobes remain deasserted and A0-A15 and X/$\overline{Y}$ do not change from their previous state. Both $\overline{PS}$ and $\overline{DS}$ will be deasserted (they do not change between two external accesses to the same memory space) indicating that no external memory access is occurring. If $\overline{BR}$ has been asserted, then the bus signals will be three-stated according to the timing information in this data sheet.

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
115	Delay from $\overline{BR}$ Assertion to $\overline{BG}$ Assertion (see Note 1)	2*cyc+tch	4*cyc+tch+20	2*cyc+tch	4*cyc+tch+15	2*cyc+tch	4*cyc+tch+13	ns
	(see Note 2)	cyc+tch	4*cyc+tch+cyc*WS+20	cyc+tch	4*cyc+tch+cyc*WS+15	cyc+tch	4*cyc+tch+cyc*WS+13	ns
	(see Note 3)	cyc+tch	6*cyc+tch+2*cyc*WS+20	cyc+tch	6*cyc+tch+2*cyc*WS+15	cyc+tch	6*cyc+tch+2*cyc*WS+13	ns
	(see Note 4)	Infinity	—	Infinity	—	Infinity	—	ns
	(see Note 5)	tch+4	cyc+tch+30	tch+3	cyc+tch+23	tch+3	cyc+tch+19	ns
116	Flags Input Hold Time After RXC Falling Edge Deassertion	2*cyc	4*cyc+20	2*cyc	4*cyc+15	2*cyc	4*cyc+13	ns
117	$\overline{BG}$ Deassertion Duration	2*cyc-10	—	2*cyc-8	—	2*cyc-6	—	ns
118	Delay from Address, Data, and Control Bus High Impedance to $\overline{BG}$ Assertion	0	—	0	—	0	—	ns
119	Delay from $\overline{BG}$ Deassertion to Address, Data, and Control Bus Enabled	—	tch-10	—	tch-8	—	tch-6	ns
120	Address Valid to $\overline{WR}$ Assertion WS=0	tcl-9	tcl+5	tcl-7	tcl+5	tcl-5.5	tcl+5	ns
	WS>0	cyc-9	cyc+5	cyc-7	cyc+5	cyc-5.5	cyc+5	ns
121	$\overline{WR}$ Assertion Width WS=0	cyc-9	—	cyc-7	—	cyc-5.0	—	ns
	WS>0	WS*cyc+tcl-9	—	WS*cyc+tcl-7	—	WS*cyc+tcl-5.0	—	ns
122	$\overline{WR}$ Deassertion to Address Not Valid	tch-12	—	tch-9	—	tch-7.5	—	ns
123	$\overline{WR}$ Assertion to Data Out Valid WS=0	tch-9	tch+10	tch-7	tch+8	tch-5.5	tch+6.5	ns
	WS>0	0	10	0	8	0	6.5	ns
124	Data Out Hold Time from $\overline{WR}$ Deassertion (The maximum specification is periodically sampled, and not 100% tested.)	tch-9	tch+7	tch-7	tch+6	tch-5.5	tch+4.5	ns
125	Data Out Setup Time to $\overline{WR}$ Deassertion (see Note 6) WS=0	tcl-5	—	tcl-5	—	tcl-5	—	ns
	WS>0	WS*cyc+tcl-5	—	WS*cyc+tcl-5	—	WS*cyc+tcl-5	—	ns
126	$\overline{RD}$ Deassertion to Address Not Valid	tch-9	—	tch-7	—	tch-5.5	—	ns

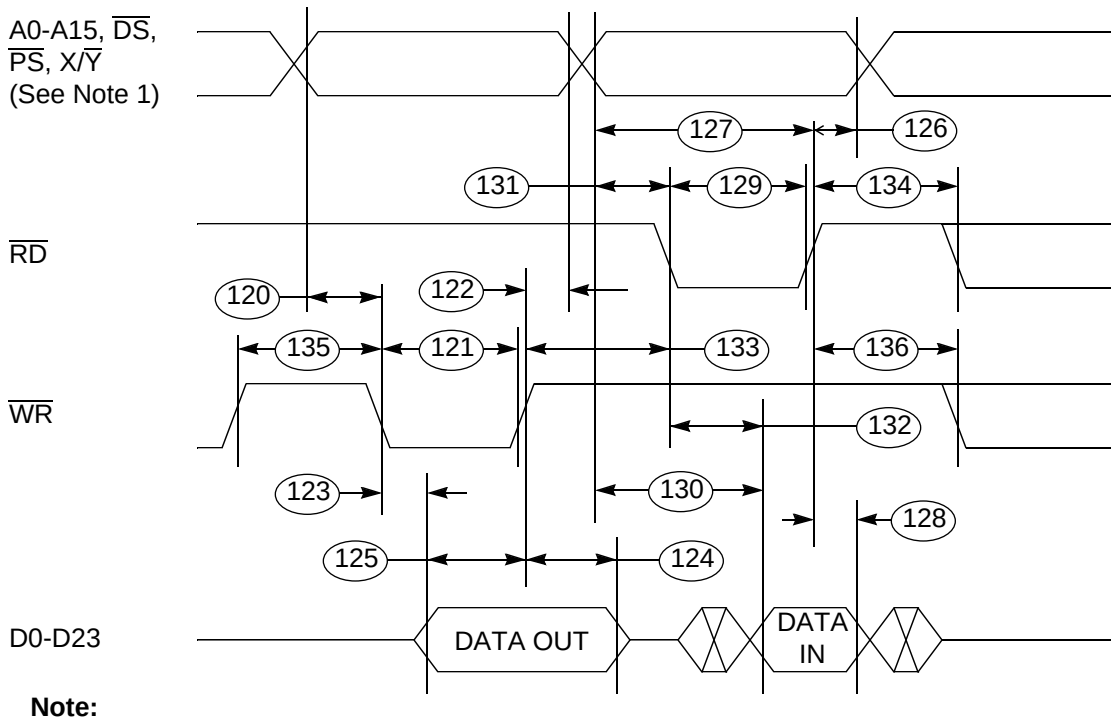
Num	Characteristics		20.5 MHz		27 MHz		33 MHz		Unit
			Min	Max	Min	Max	Min	Max	
127	Address Valid to $\overline{RD}$ deassertion	WS = 0 WS > 0	cyc+tcl-8 ((WS+1)$*$ cyc)+tcl-8	— —	cyc+tcl-6 ((WS+1)$*$ cyc)+tcl-6	— —	cyc+tcl-6 ((WS+1)$*$ cyc)+tcl-6	— —	ns ns
128	Input Data Hold Time to $\overline{RD}$ Deassertion		0	—	0	—	0	—	ns
129	$\overline{RD}$ Assertion Width	WS = 0 WS > 0	cyc-9 ((WS+1)* cyc)-9	— —	cyc-7 ((WS+1)* cyc)-7	— —	cyc-5.5 ((WS+1)* cyc)-5.5	— —	ns ns
130	Address Valid to Input Data Valid	WS = 0 WS > 0	— —	cyc+tcl-18 ((WS+1)$*$ cyc)+tcl-18	— —	cyc+tcl-14 ((WS+1)$*$ cyc)+tcl-14	— —	cyc+tcl-11 ((WS+1)$*$ cyc)+tcl-11	ns ns
131	Address Valid to $\overline{RD}$ Assertion		tcl-9	tcl+5	tcl-7	tcl+5	tcl-5.5	tcl+5	ns
132	$\overline{RD}$ Assertion to Input Data Valid	WS=0 WS>0	— —	cyc-14 ((WS+1)* cyc)-14	— —	cyc-11 ((WS+1)* cyc)-11	— —	cyc-9 ((WS+1)* cyc)-9	ns ns
133	$\overline{WR}$ Deassertion to $\overline{RD}$ Assertion		cyc-15	—	cyc-12	—	cyc-10	—	ns
134	$\overline{RD}$ Deassertion to $\overline{RD}$ Assertion		cyc-10	—	cyc-8	—	cyc-6.5	—	ns
135	$\overline{WR}$ Deassertion to $\overline{WR}$ Assertion	WS=0 WS>0	cyc-15 cyc+tch-15	— —	cyc-12 cyc+tch-12	— —	cyc-10 cyc+tch-10	— —	ns ns
136	$\overline{RD}$ Deassertion to $\overline{WR}$ Assertion	WS=0 WS>0	cyc-10 cyc+tch-10	— —	cyc-8 cyc+tch-8	— —	cyc-6.5 cyc+tch-6.5	— —	ns ns

Notes:

1. With no external access from the DSP.
2. During external read or write access.
3. During external read-modify-write access.
4. During the STOP mode the external bus will not be released and $\overline{BG}$ will not go low. However, if the bus is released ($\overline{BG}$ = 0) and the STOP instruction is executed while $\overline{BG}$ = 0 then the bus will remain released while the DSP is in the stop state and $\overline{BG}$ will remain low.
5. During the WAIT mode the $\overline{BR}$/$\overline{BG}$ circuits remain active.
6. Typical values at 5V are:
   at 20.5 MHz and WS=0, Min = tcl-4
   at 20.5 MHz and WS>0, Min = WS$*$cyc+tcl-4
   at 27 MHz and WS=0, Min = tcl-3
   at 27 MHz and WS>0, Min = WS$*$cyc+tcl-3
   at 33 MHz and WS=0, Min = tcl-2.5
   at 33 MHz and WS>0, Min = WS$*$cyc+tcl-2.5



Async. Bus Figure 1. Bus Request / Bus Grant Timing



Note:
1. During Read-Modify-Write instructions and internal instructions, the address lines do not change state.

Async. Bus Figure 2. External Bus Asynchronous Timing

DSP56001 Electrical Characteristics

AC Electrical Characteristics - External Bus Synchronous Timing

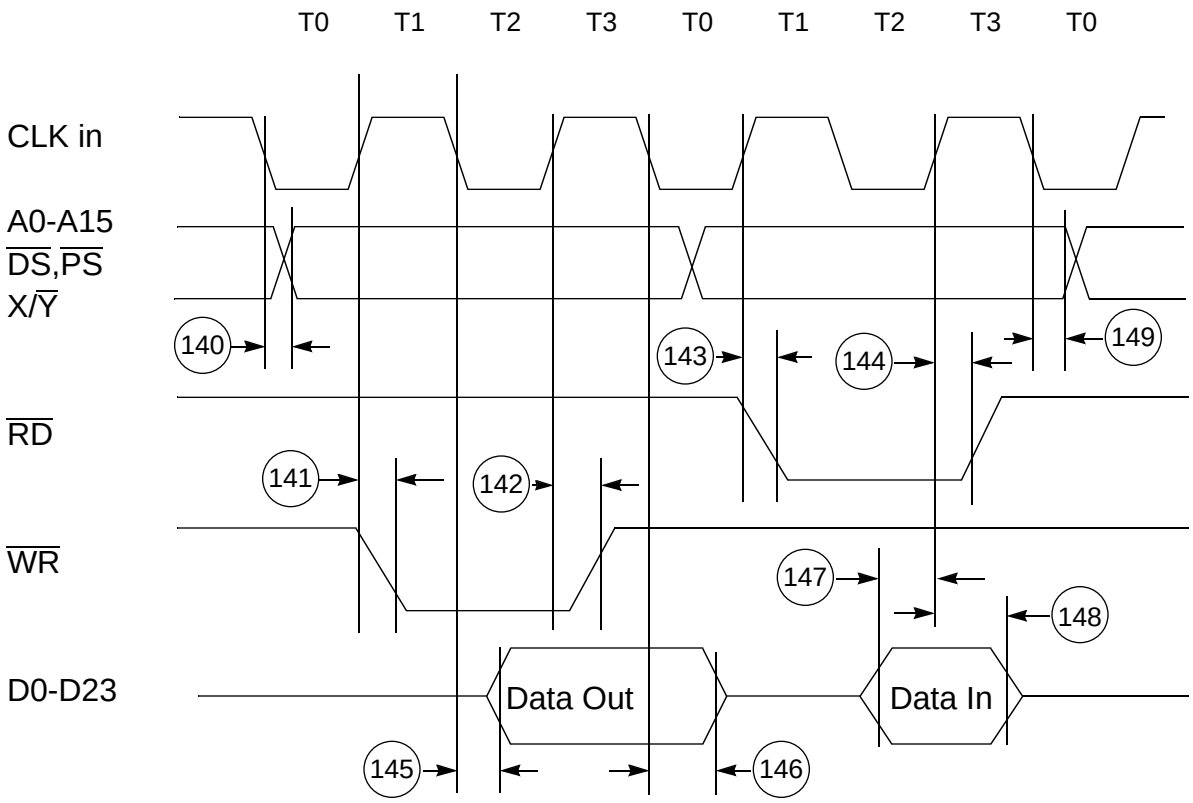
Vcc = 5.0 Vdc ± 10%; T_J = -40 to 105° C at 20.5 MHz 27 MHz

Vcc = 5.0 Vdc ± 5%; T_J = -40 to 105° C at 33 MHz

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
140	Clk Low Transition To Address Valid	—	24	—	19	—	19	ns
141	Clk High Transition To $\overline{WR}$ Assertion (see Note 2) WS = 0 WS > 0	0 0	19 tch+19	0 0	15 tch+15	0 0	17 tch+17	ns ns
142	Clk High Transition To $\overline{WR}$ Deassertion	5	21	5	16	5	13	ns
143	Clk High Transition To $\overline{RD}$ Assertion	0	19	0	15	0	16	ns
144	Clk High Transition To $\overline{RD}$ Deassertion	5	17	5	13	4.5	10.5	ns
145	Clk Low Transition To Data-Out Valid	—	25	—	19	—	19	ns
146	Clk Low Transition To Data-Out Invalid (see Note 3)	5	—	4	—	3.5	—	ns
147	Data-In Valid To Clk High Transition (Setup)	0	—	0	—	0	—	ns
148	Clk High Transition To Data-In Invalid (Hold)	12	—	12	—	13	—	ns ns
149	Clk Low To Address Invalid (see Note 3)	3	—	3	—	3	—	ns

Notes:

1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition.
2. WS are wait state values specified in the BCR.
3. Clk low to data-out invalid (spec. 146) and Clk low to address invalid (spec. 149) indicate the time after which data/address are no longer guaranteed to be valid.



Sync. Bus Figure 1. DSP56001 Synchronous Bus Timing

Note: During Read-Modify-Write Instructions, the address lines do not change states.

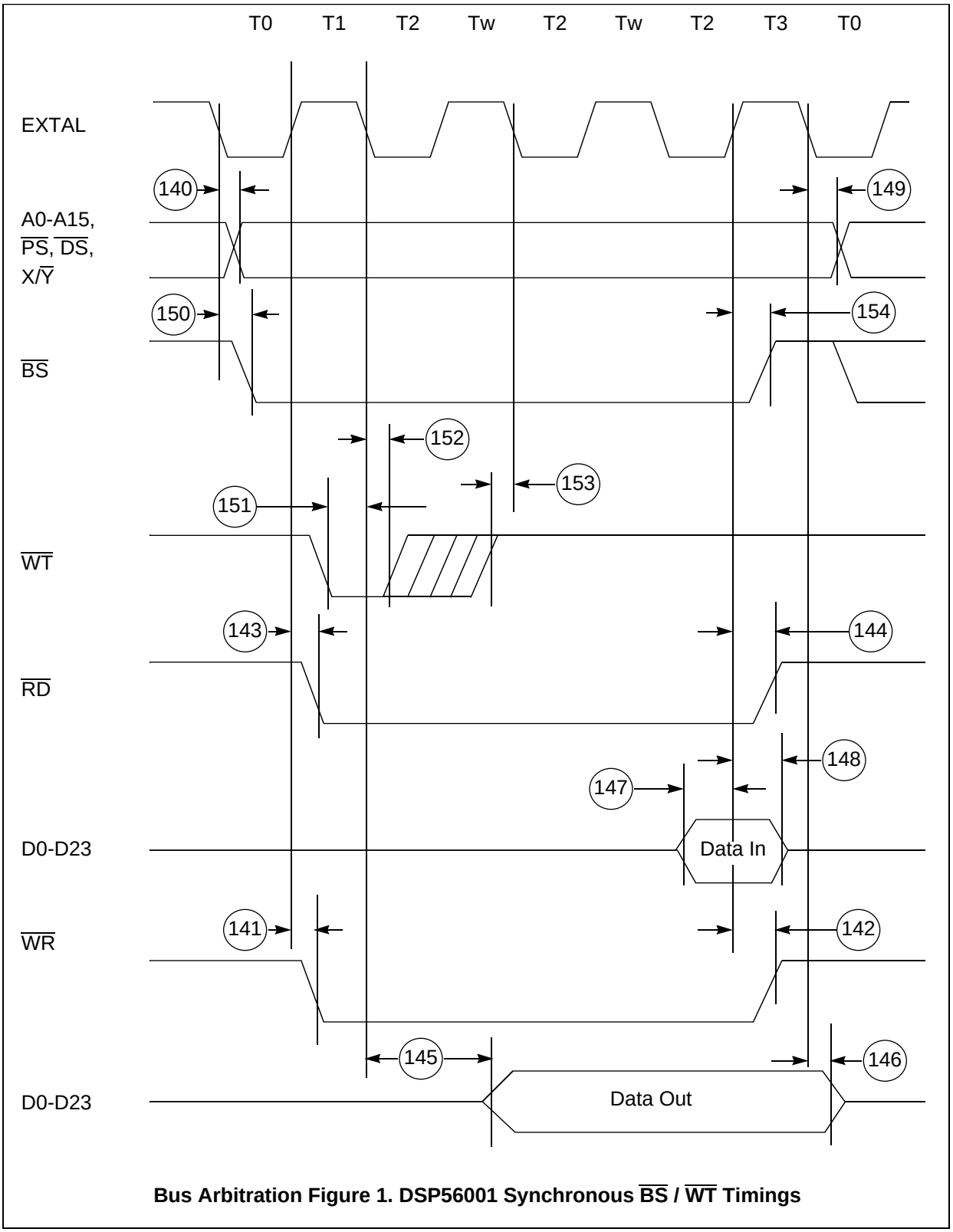
DSP56001 Electrical Characteristics

AC Electrical Characteristics - Bus Strobe / Wait Timing

Num	Characteristics	20.5 MHz		27 MHz		33 MHz		Unit
		Min	Max	Min	Max	Min	Max	
150	Clk Low Transition To $\overline{BS}$ Assertion	4	24	3	19	2.5	19	ns
151	$\overline{WT}$ Assertion To Clk Low Transition (setup time)	4	—	3	—	2.5	—	ns ns
152	Clk Low Transition To $\overline{WT}$ Deassertion For Minimum Timing	14	cyc-8	11	cyc-6	12	cyc-5	ns
153	$\overline{WT}$ Deassertion To Clk Low Transition For Maximum Timing (2 wait states	8	—	6	—	5	—	ns
154	Clk High Transition To $\overline{BS}$ Deassertion	5	26	4	20	3.5	19	ns
155	$\overline{BS}$ Assertion To Address Valid	-2	10	-2	8	-2	6.5	ns
156	$\overline{BS}$ Assertion To $\overline{WT}$ Assertion (see Note 2)	0	cyc-15	0	cyc-11	0	cyc-10	ns
157	$\overline{BS}$ Assertion To $\overline{WT}$ Deassertion (See Note 2 and Note 4) WS $\leq$ 2 WS $\geq$ 2	cyc (WS-1) $*$cyc	2*cyc-15 WS*cyc -15	cyc (WS-1) $*$cyc	2*cyc-11 WS*cyc -11	cyc+4 (WS-1) $*$cyc+4	2*cyc-10 WS*cyc -10	ns ns
158	$\overline{WT}$ Deassertion To $\overline{BS}$ Deassertion	cyc+tcl	2$*$cyc+tcl +23	cyc+tcl	2$*$cyc+tcl +17	cyc+tcl	2$*$cyc+tcl +15	ns
159	Minimum $\overline{BS}$ Deassertion Width For Consecutive External Accesses	tch-7	—	tch-6	—	tch-4.5	—	ns
160	$\overline{BS}$ Deassertion To Address Invalid (see Note 3)	tch-10		tch-8		tch-6.5		
161	Data-In Valid to $\overline{RD}$ Deassertion (Set Up)	16	—	12	—	10	—	ns

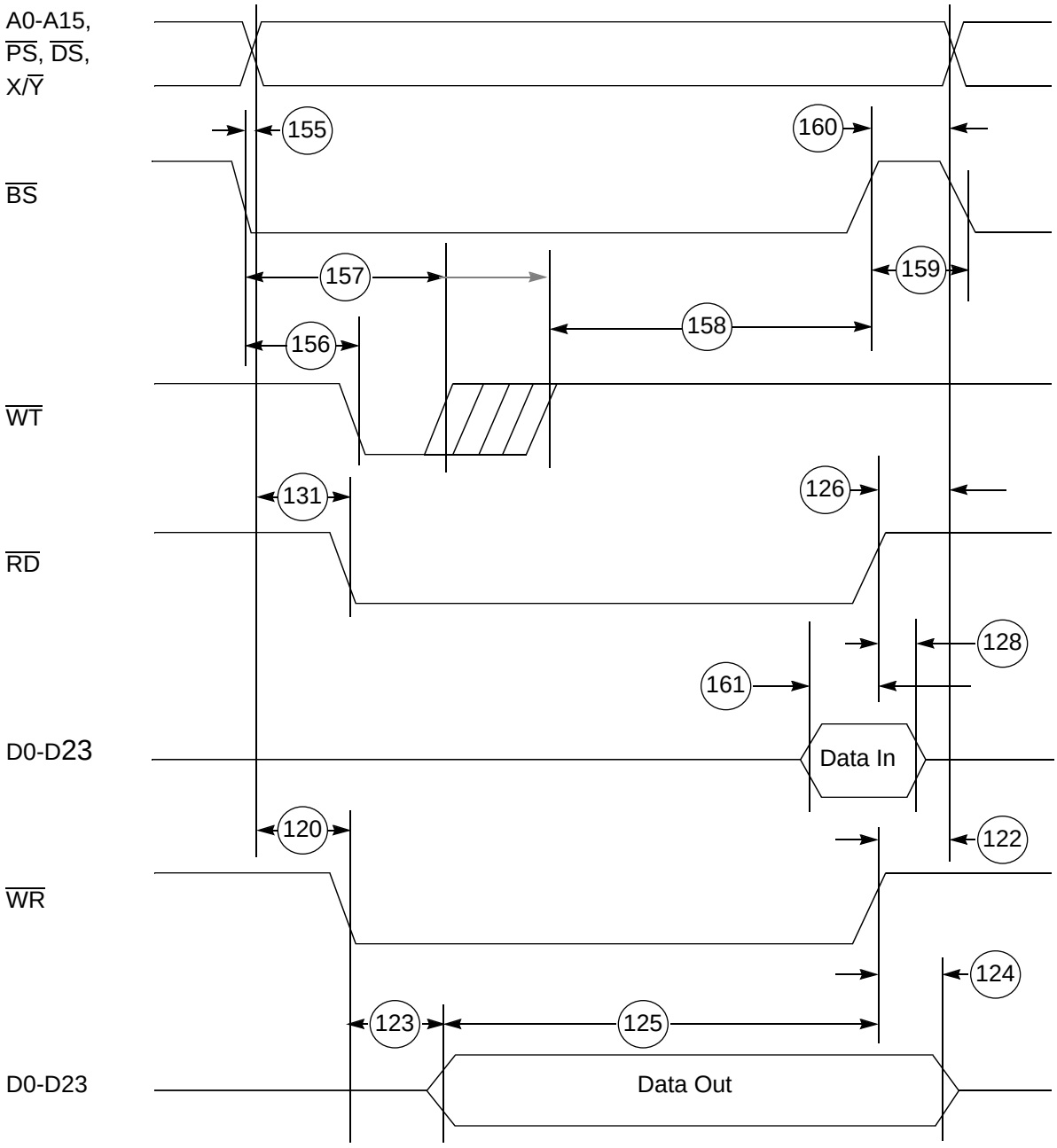
Note:

1. AC timing specifications which are referenced to a device input signal are measured in production with respect to the 50% point of the respective input signal's transition.
2. If wait states are also inserted using the BCR and if the number of wait states is greater than 2, then specification numbers 156 and 157 can be increased accordingly.
3. $\overline{BS}$ deassertion to address invalid indicates the time after which the address are no longer guaranteed to be valid.
4. The minimum number of wait states when using $\overline{BS}$/$\overline{WT}$ is two (2).
5. For read-modify-write instructions, the address lines will not change states between the read and the write cycle. However, $\overline{BS}$ will deassert before asserting again for the write cycle. If wait states are desired for each of the read and write cycle, the $\overline{WT}$ pin must be asserted once for each cycle.



Bus Arbitration Figure 1. DSP56001 Synchronous $\overline{BS}$ / $\overline{WT}$ Timings

Note: During Read-Modify-Write Instructions, the address lines do not change state. However, $\overline{BS}$ will deassert before asserting again for the write cycle.



Bus Arbitration Figure 2. DSP56001 Asynchronous $\overline{BS}$ / $\overline{WT}$ Timings

Note: During Read-Modify-Write Instructions, the address lines will not change states. However, $\overline{BS}$ will deassert before asserting again for the write cycle.

DSP56001 Electrical Characteristics