ATARI XL Expansion System

Technical Specification

Revision A

5/11/84

Contents

1.0 Introduction

The Expansion Box is an extension device providing support of expansion cards for the Atari Computer line. This device provides Atari systems with expansion and enhancement. The bus enables the consumer to connect a variety of different devices to the Expansion Box Interface (E.B.I.). Some devices are listed below.

1) RAM EXPANSION
2) SERIAL/PARALLEL INTERFACE
3) Z-80 PROCESSOR
4) 80-COLUMN VIDEO MONITOR INTERFACE
5) HOBBYIST PROTOTYPING CARD

1.1 Product Objectives

A. To provide system expansion.
B. To provide multiple device access to the Parallel Bus Interface (P.B.I.)
C. To provide an interface standard for encouraging peripheral manufacturers to develop P.B.I. Devices.

2.0 Product Description

2.1 Mechanical

2.1.1 Appearance

The Expansion Box matches the styling of the current XL product line. The Box has all connections to devices and power in the rear of the box. A flat cable (connected to the front of the box) connects the Expansion Box to all PBI-equipped computers.

2.1.2 Design Concepts

The Expansion box requires less than one square foot of table space. The top is easily removable so the user can access the option cards. The Box supports five 9 by 5 inch option cards (see figure 1). To remove the top of the box, the AC adapter must be unplugged from the box.

FIGURE 1 Option Card Size

2.2 Electrical

2.2.1 Architectural Overview

The expansion box contains a triple-output power supply providing regulated +12 volts and -12 volts and +10 volts unregulated. Also provided is a half-wave rectified AC waveform (for power-line frequency reference only) and +5 volts (for reference only).

The address bus, data bus and control lines are buffered by the expansion box and bussed to the five edge connectors provided.

2.2.2 Expansion Bus Interface

2.2.2.1 Connector

The Expansion Box Interface signals are accessible through a 50-pin connector. This connector is an AMP type 2-530843-9 (see figure 2). It mates to a standard card edge with gold plated fingers at .100 inch centers.

FIGURE 2 Card Edge Connector

+10V	2	1	+10V
AUDIO IN	4	3	EXTSEL'
GND	6	5	EXTENB
MPD'	8	7	REF
IRQ'	10	9	RDY'
RESET'	12	11	AC
ABUFFSEL'	14	13	CARDSEL'
-12V	16	15	BR/W'
GND	18	17	A15
BPHASE2	20	19	A14
GND	22	21	A13
+5V REF	24	23	A12
Reserved	26	25	A11
Reserved	28	27	A10
Reserved	30	29	A9
DBUFSEL'	32	31	A8
D7	34	33	A7
D6	36	35	A6
D5	38	37	A5
D4	40	39	A4
D3	42	41	A3
D2	44	43	A2
D1	46	45	A1
D0	48	47	A0
+12V	50	49	COMPGNDRET

FIGURE 3 Connector Pin-Out Top View

2.2.2.2 Signals Types

Shown in figure 3 is the pin-out of the connector looking into the expansion box. The signal pin numbers and signal names are described below.

Pin 47	A0	Address Line 0 (Output) ==> Address line 0 is a buffered output from the micro-processor.
Pin 45	A1	Address Line 1 (Output) ==> Address line 1 is a buffered output from the micro-processor.
Pin 43	A2	Address Line 2 (Output) ==> Address line 2 is a buffered output from the micro-processor.
Pin 41	A3	Address Line 3 (Output) ==> Address line 3 is a buffered output from the micro-processor.
Pin 39	A4	Address Line 4 (Output) ==> Address line 4 is a buffered output from the micro-processor.
Pin 37	A5	Address Line 5 (Output) ==> Address line 5 is a buffered output from the micro-processor.
Pin 35	A6	Address Line 6 (Output) ==> Address line 6 is a buffered output from the micro-processor.
Pin 33	A7	Address Line 7 (Output) ==> Address line 7 is a buffered output from the micro-processor.
Pin 31	A8	Address Line 8 (Output) ==> Address Line 8 is a buffered output from the micro-processor.
Pin 29	A9	Address Line 9 (Output) ==> Address line 9 is a buffered output from the micro-processor.
Pin 27	A10	Address Line 10 (Output) ==> Address line 10 is a buffered output from the micro-processor.

Pin 25	A11	Address Line 11 (Output) ==> Address line 11 is a buffered output from the microprocessor.
Pin 23	A12	Address Line 12 (Output) ==> Address line 12 is a buffered output from the microprocessor.
Pin 21	A13	Address Line 13 (Output) ==> Address line 13 is a buffered output from the microprocessor.
Pin 19	A14	Address Line 14 (Output) ==> Address line 14 is a buffered output from the microprocessor.
Pin 17	A15	Address Line 15 (Output) ==> Address line 15 is a buffered output from the microprocessor.
Pin 48	D0	Data Line 0 (Bi-directional) ==> Data line 0 is a buffered bi-directional data line.
Pin 46	D1	Data Line 1 (Bi-directional) ==> Data line 1 is a buffered bi-directional data line.
Pin 44	D2	Data line 2 (Bi-directional) ==> Data line 2 is a buffered bi-directional data line.
Pin 42	D3	Data Line 3 (Bi-directional) ==> Data line 3 is a buffered bi-directional data line.
Pin 40	D4	Data Line 4 (Bi-directional ==> Data line 4 is a buffered bi-directional data line.
Pin 38	D5	Data Line 5 (Bi-directional) ==> Data line 5 is a buffered bi-directional data line.
Pin 36	D6	Data Line 6 (Bi-directional) ==> Data line 6 is a buffered bi-diurectional data line.
Pin 34	D7	Data Line 7 (Bi-directional_ ==> Data line 7 is a buffered bi-directional data line.

Pins 1,2	+10V	+10 Volts, Unregulated
Pin 3	EXTSEL'	External Select (Input) ==> This open collector line is generated internally by the Expansion Box Device (E.B.D.). This signal should be active low whenever EXTENB is active and the E.B.D. is selected and there is a valid E.B.D. address on the bus. EXTSEL' causes a CAS' inhibit on the main board allowing a remapping process. Although E.B.D. can be mapped in any VALID RAM location, these devices should follow the ATARI guidelines for E.B.D. locations so future ATARI devices can be used. The drive device should be capable of sinking 10 mA.
Pin 4	AUDIO	Audio In (Input) ==> This line is tied directly to the audio summation network of the computer. The audio signal input is 100mV peak to peak with 4.7K ohm load impedance.
Pin 5	EXTENB	External Decoder Enable (Output) ==> This output goes high when there is a valid RAM access. Any E.B.D. can map during a valid EXTENB but the E.B.D. should only map in according to ATARI specified address locations.
Pin 6	GND	Ground
Pin 18	GND	Ground
Pin 22	GND	Ground
Pin 7	REF'	Refresh (Output) ==> This output can be for refresh timing on dynamic memories connected to the E.B.I.
Pin 8	MPD'	Math Pack Disable (Input) ==> This open collector input is used to disable the math pack section of the OS ROM (D800H-DFFFH). This should be done when the E.B.D. is selected and has a handler resident. The driving device should be capable of sinking 10 mA.

Pin 9	RDY	Ready (Input) ==> This open collector input signal allows the E.B.D. to halt the microprocessor ONLY during read cycles. Driving this input low will extend the read cycle for slow peripherals. The driving device should be capable of sinking 10 mA.
Pin 10	IRQ'	Interrupt Request (Input) ==> This open collector line creates an interrupt on the microprocessor. The interrupt can then invoke the handler ROM or other service routines for the E.B.D. The driving device should be capable of sinking 10 mA.
Pin 11	AC	The half-wave rectified AC signal from the power supply bridge. May be used as an unfiltered line-frequency reference.
Pin 12	RESET'	Reset (Output) ==> Reset is an active low signal which occurs either on power-up or by depressing the reset key on the computer.
Pin 14	ABUFFSEL'	Buffer Select (Input) ==> This signal, when driven high disables (tristates) the address lines from the computer.
Pin 13	CARDSEL'	(output) ==> This signal enables the E.B.D. to respond to the hardware protocol. In the 1090 it will always be grounded. In future Atari products it will be an address space select line for processors which have an address space in excess of 64K.
Pin 15	BR/W'	Buffered Read/Write (Output) ==> This output is active high for a read cycle and active low for a write cycle.
Pin 16	-12V	-12 Volts, Regulated
Pin 20	BPHASE2	Buffered Phase 2 Clock (Output) ==> This clock output line is a buffered phase 2 clock from the processor.
Pin 24	+5V REF	This is a +5 VDC regulated reference. Expansion box cards should not draw mo than 10 mA maximum from this reference.
Pins 26,28,30		Reserved for future use.

Pin 32 DBUFSEL' Data Buffer Select (Input) ==> This signal, when driven low enables the data bus transceivers for data to and from the computer.

Pin 49 COMPGNDRET Computer Ground Return is a ground connection only through the flat cable connector and is otherwise isolated.

Pin 50 +12V +12 Volts, Regulated

2.2.2.3 Interface Requirements

For peripherals to interface through the E.B.I. to the computer, the following requirements must be followed.

2.2.2.3.1 D.C. Characteristics

All E.B.I. outputs have the drive capability of 24 mA at logic 0 (I_{OL}) and -6 mA at logic 1 (I_{OH}).

All E.B.I. open collector input lines must be able to sink 10 mA (min) at .4 V(max).

All E.B.I. non-open collector input lines except AUDIO must have the drive capability of 24 mA at logic 0 (I_{OL}) and -6 mA at logic 1 (I_{OH}).

All E.B.I. signals except AUDIO will be at standard TTL logic levels.

The AUDIO input line must drive a 4.7 KOhm source impedance with a 100 mV peak to peak signal.

Each expansion box card should not load any E.B.I. output line with more that three standard TTL loads.

2.2.2.3.2 A.C. Characteristics

All specifications are referenced to the standard 2 MHz 6502 specifications.

The signal PHASE2 is the 6502 clock at the processor.

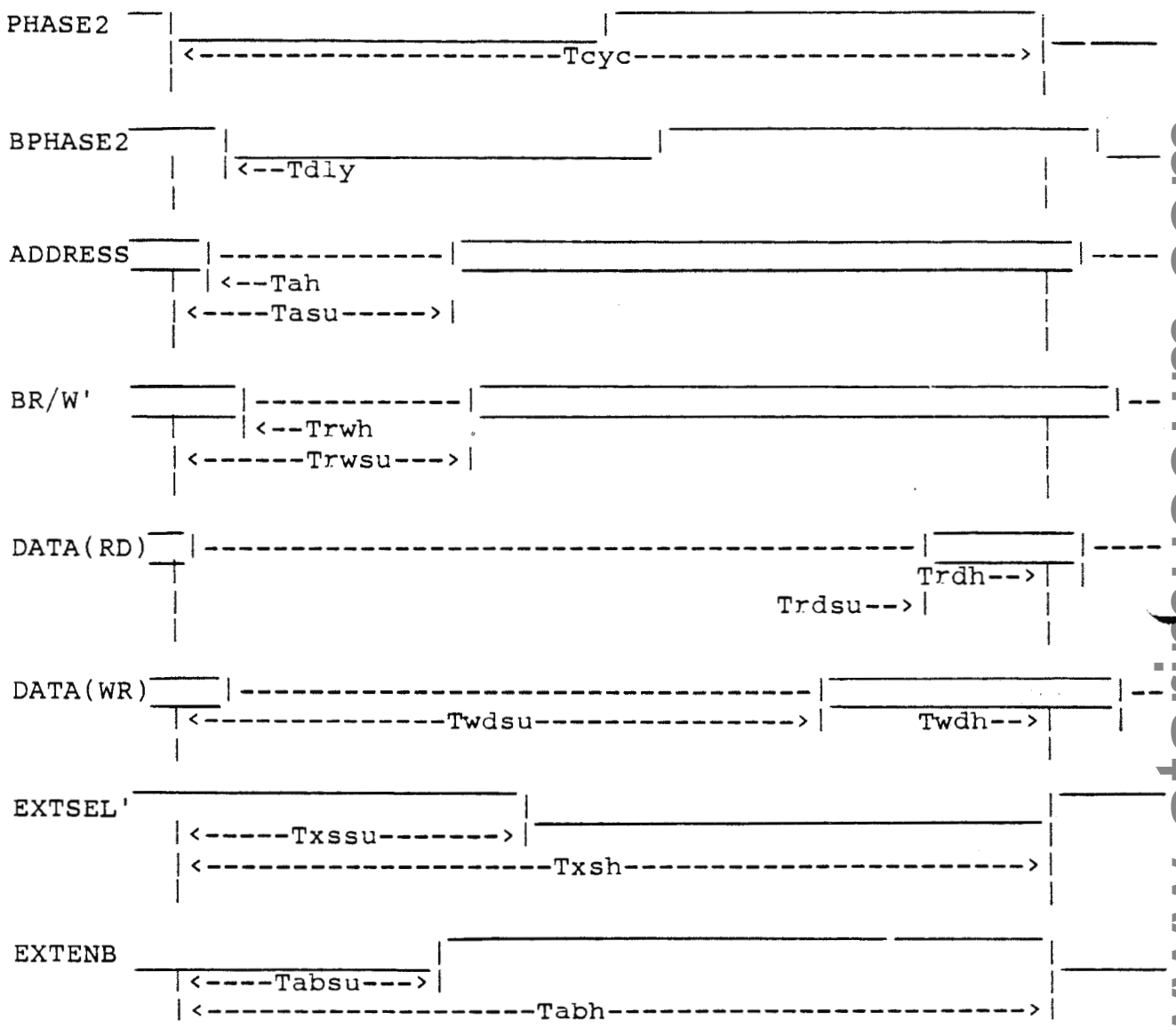

FIGURE 4 Timing Diagram

PARAMETER	SYMBOL	MIN	MAX	UNITS
BPHASE2	Tcyc	558	559	ns
Delay - 6502 PHASE2 to BPHASE2	Tdly	5	31	ns
Address hold time	Tah	5		ns
Address setup time	Tasu		177	ns
R/W' hold time	Trwh	38		ns
R/W' setup time	Trwsu		186	ns
Read Data setup time	Trdsu	72		ns
Read Data hold time	Trdh	7		ns
Write Data setup time	Twdsu		422	ns
Write Data hold time	Twdh	33		ns
EXTSEL' setup time	Txssu		250	ns
EXTSEL' hold time	Txsh	558		ns
EXTENB setup time	Tabsu		195	ns
EXTENB hold time	Tabh	558		ns

TABLE 1 Parameter Table

2.2.2.3.3 Materials Requirements

Contact fingers shall be plated with nickel of the low-stress type, Class II per federal specification QQ-N290A. Nickel plate thickness shall be 100 +/- 25 microinches. The nickel plating shall be overplated with gold type II (23+ karat), 15 microinches mininimum (130-200 knoop hardness) or 10 microinches minimum (201 or over knoop hardness) Impurities shall not exceed .1 %, not including metallic hardeners. Roughness shall be less than 50 microinches.

2.2.2.4 Hardware Device Protocol

The E.B.D.s have the following characteristics:

1. The interface between the E.B.D. and the CPU is defined through the handler/OS resident in the OS ROM. The OS can support 8 devices at one time with only one enabled during any given interval.

2. Every E.B.D. has a unique handler that resides in the CPU memory from D800H-DFFFH. The ROMs containing the code for these handlers are physically resident on the respective E.B.D.s. To access this handler, the math pack must be disabled with MPD'. When the math pack is disabled (this should happen whenever the E.B.D. is selected and has a external handler) the computer will generate EXTENB for the math pack area. The E.B.D. must then generate the correct EXTENB/EXTSEL' protocol. If the device does not generate EXTSEL' the CPU will access (in the 64K computers) an unused area of RAM. This area should not be used since all computers of this series do not have that area of ram.

3. The location D1FFH in the CPU memory map is reserved for passing control information between the CPU and the E.B.D.s. The CPU selects one of the devices by writing a "1" into the desired bit in location D1FFH. The device can be deselected by writing a "0" into the desired bit.

7	6	5	4	3	2	1	0
D7	D6	D5	D4	D3	D2	D1	D0

The CPU can access 8 devices, but only one of the devices may be active at a time.

If the IRQ' line is pulled "low" the CPU can read the status for location D1FFH and locate the requesting E.B.D. A "1" in a bit Ix (where x=0 to 7) corresponds to an interrupt in E.B.D. x. If the bit is a "0" then the device has not caused the interrupt.
The E.B.D.must clear the interrupt flag when the interrupt is being serviced.

7	6	5	4	3	2	1	0
I7	I6	I5	I4	I3	I2	I1	I0

4. An E.B.D. should assert MPD' only when it is selected. An E.B.D. should assert EXTSEL' only when it is selected and if EXTENB is asserted.

5. An E.B.D. may respond to any selects D0 through D7. It is recommended that the E.B.D.s have configuration switches to allow them to respond to any one of the selects. Some of the computer systems use the E.B.I. to support internal devices; therefore the user should check each manual for device locations. If the system has devices in specific locations, those are reserved in that computer.

6. An E.B.D. handler may respond to addresses in the region D800H-DFFFH only when it is selected.

7. A peripheral may respond to addresses in the region D100H to D1AFH only when selected.

8. The E.B.D.s will have priority over the SIO peripherals when they are addressed generically.

9. Data Transfer between the CPU and the E.B.D. is under the control of the peripheral handler for the E.B.D.s.

10. The CPU address space from D600H to D7FFH is reserved for E.B.I. devices as follows:

Device	Range	Size
D0	D600H-D61FH	32 Bytes
	D620H-D63FH	Reserved for modems
D1	D640H-D67FH	64 Bytes
D2	D680H-D6BFH	64 Bytes
D3	D6C0H-D6FFH	64 Bytes
D4	D700H-D73FH	64 Bytes
D5	D740H-D77FH	64 Bytes
D6	D780H-D7BFH	64 Bytes
D7	D7C0H-D7FFH	64 Bytes

The 800XL will not provide CPU RAM in this address space. The 600XL has no internal RAM in this address space. The 1450XL does allow access to internal CPU RAM in this address space. E.B.D.s should provide this RAM on the E.B.D. or be restricted for use only on the 1450XL.

2.2.3 Power Supply

The power supply is comprised of an external AC adapter capable of providing 40 VA at 9.5 vAC to the Expansion Box and an internal rectifier/ filter/regulator system. This system provides:

+10 vDC UNREGULATED(+40% or -15%) at .5 A per card slot
+12 vDC REGULATED(+ or - 4%) at 30 mA per card slot
-12 vDC REGULATED(+ or - 4%) at 30 mA per card slot
+5VREF REGULATED(+ or - 4%) as a reference only
AC - a 60 Hz reference only

Total supply current capacity is five times the per card slot amounts.

It is recommended that the Expansion Box NOT be operated with the cover removed for safety reasons and to comply with radiated emissions standards.

2.4 Product Performance

This section specifies the projected performance of the Expansion Box. Environmental and reliability information is included.

2.4.1 Environmental

Operating Environment

Temperature =
  Maximum: 40 degrees C
  Minimum: 10 degrees C
Humidity =
  Maximum: 90% R.H. (Non Condensing)
  Minimum: 15% R.H.
Altitude =
  Maximum: 3000 Meters (9840 feet) (720 millibars)
  Minimum: 60 Meters (-197 feet) below sea level

Non-Operating Environment

Temperature =
  Maximum: 60 Degrees C
  Minimum: -30 Degrees C
Humidity =
  Maximum: 90% R.H. Should condensing occur, unit must be dried off before operation.
  Minimum: 0% R.H.
Altitude =
  Same as operating

2.4.2 Endurance Levels

ESD Susceptibility

No product damage up to a 25KV discharge or data loss up to a 15 KV discharge at any point accessible to the user except the connectors. (ESD Product Spec. C021703)

Vibration

Operation:	.1g + or - 10% 5 to 500Hz
Resonance Search:	Sine scan 5-100 Hz dwell on resonances 1.0g for 10 minutes.
Transportation:	100 to 300 cycles per minute two directions, 90 degrees apart, 30 minutes; each frequency to be such as to raise package from the table 0.06 in., acceleration to be 1.0g (min). No damage should result.
Impact Test:	Free fall distance of 24 in. on corner, edge, and all 6 faces. No damage should occur to a packed unit.
Random Vibration:	0.04g2/Hz, 15 minutes; 10 to 1000 Hz, 6.3g RMS.
Thermal Shock:	10 degrees C for 3 hours, power on, raise temperature 56 degrees per minute to 45 degrees C for 5 hours; power off, drop temperature 5 degrees C per minute to 10 degrees C. Repeat cycle 5 times; no damage.

The MTBF for the Expansion Box is 8000 hours continuous power-on at 25 degrees C.

The MTTR for the unit is 10 minutes.

2.4.4 Compliances

UL 114 & UL 94HB
CSA C22.2 No. 154
FCC Docket 20780, Part 15, Subpart J, Class B

3.0 Notes

3.1 RAM 64KMR

The RAM 64KMR module is designed to be used in the expansion box. However, it does not completely adhere to the E.B.I. protocol since it will allow RAM to be selected in lieu of the O/S (when used in the "1064 mode".)

3.2 RESERVED MEMORY LOCATIONS

The memory space from D100H to D1AFH is available for use by most applications. This space should be used by a device with the device select bit enabling its use. If the device select bit is not used, there is potential bus conflict between E.B.D.s. The remainder of the I/O space between D1B0H and D1FFH is mapped as follows:

D1B0H - D1C7H	Speech/Modem/Disc Registers
D1C8H - D1CEH	Atari Reserved
D1CFH	Alternate Interrupt Register(1450 only)
D1D0H - D1DFH	Audio Registers
D1E0H - D1E7H	Atari Reserved
D1E8H - D1EFH	Parrellel/Serial Registers
D1F0H - D1F7H	Alternate CPU Registers
D1F8H - D1FDH	80 Column Video Registers
D1FEH	RAM Bank Select Register
D1FFH	E.B.D. Select/Interrupt Register