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A	INCORP. PER ECN A0986	12/23/82	

	1200
NEXT ASSY	USED ON

DRAWN BY / DATE	Paula Shake 11/19/82
CHECKED	11-19-82
ENGINEER	11-19-82
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TITLE

ATARI 1200XL TEST SPECIFICATION

SIZE	DRAWING NO.	REV
A	C061217	A
SCALE	SHEET 1 OF 41	

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1.0 SCOPE

This specification defines the general physical and electrical requirements for the Atari 1200XL home Computer. The 1200XL is a low cost personal computer intended for use in a domestic environment. The SW-16 is an en- hanced version of the Atari 800 computer system. It is reduced in size, lower in cost, and upward compatible with the Atari 800.

2.0 REFERENCE DOCUMENTS

2.1 Atari 800 Hardware Manual (C016555)

2.2 Serial Input/Output Interface Users Handbook Part 1 and 2

2.3 DeRe Atari

2.4 Electrical Requirements for the 1200XL Keyboard (C060087)

2.5 1200XL Schematics (C060586)

2.6 The 6502 Microprocessor Manual

2.7 MC68B21 (PIA) Data Sheets

2.8 Keyboard Assembly Drawings (C060046)

2.9 6502 Software Design Manual

2.10 6502 Modified Electrical Specifications (C014806)

All documents shall be of the latest revision.

3.0 MECHANICAL SPECIFICATION

3.1 DIMENSIONS

Height: 2.7 inches (6.858 cm)
Width: 15.0 inches (38. cm)
Depth: 12.5 inches (31.75 cm)
Weight: T.B.D.

3.2 INTERFACE CONNECTOR PIN OUTS

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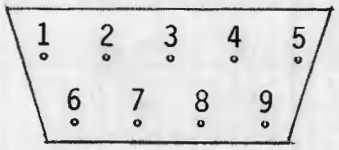
3.2.1 Controller Jack

The 1200 XL provides two controller jack interfaces. Both are functionally and electrically identical. The controller jacks are 9 pin D type male connectors.

1. (Joystick) Forward Input
2. (Joystick) Back Input
3. (Joystick) Left Input
4. (Joystick) Right Input
5. B Potentiometer Input
6. Trigger Input
7. +5 VDC
8. Ground
9. A Potentiometer Input



CONTROLLER JACK

3.2.2 Cartridge Interface

The Cartridge Interface is a 30 pin 15/30 dual readout connector.

1	$\overline{S4}$	A	RD4
2	A3	B	GND
3	A2	C	A4
4	A1	D	A5
5	AØ	E	A6
6	D4	F	A7
7	D5	H	A8
8	D2	J	A9
9	D1	K	A12
10	DØ	L	D3
11	D6	M	D7
12	$\overline{S5}$	N	A11
13	+5VDC	P	A10
14	RD5	R	R/$\overline{W}$
15	$\overline{CCTL}$	S	BØ2

3.2.3 Monitor Interface

The Monitor Interface is a 5 pin din connector.

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Pin 1: Composite Luminance - This signal contains the luminance and sync information but not the chrominance information. It is a 0 to 1 vac signal. This output has an impedance of 75 OHMS (looking into the pin).

Pin 2: Ground - Monitor Reference

Pin 3: Mono Audio Output - This is a 1V P-P AC signal. This output has an impedance of 1.8KΩ(looking into the pin).

Pin 4: Composite Video - This signal contains the luminance, chromnance, and sync information. It is a 0 to +1V AC signal. This output has an output impedance of 75 OHMS (looking into the pin).

Pin 5: No Connection

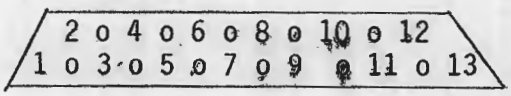
Monitor Interface

3.2.4 T.V. Interface

The 1200 XL provides an R.F. modulated output for direct connec- tion to a T.V. set. The R.F. output is available through a phono plug.

3.2.5 Serial I/O Interface

1	CLOCK IN	8	Motor Control
2	CLOCK OUT	9	PROCEED
3	DATA INTO COMPUTER	10	+5VDC/READY
4	GND	11	AUDIO IN
5	DATA OUT OF COMPUTER	12	NOT USED
6	GND	13	INTERRUPT
7	COMMAND		



SERIAL I/O INTERFACE

REV	REVISIONS DESCRIPTION	DATE	APPROVED

4.0 ENVIRONMENTAL SPECIFICATIONS

4.1 OPERATING ENVIRONMENT

Temperature: 50°F to 112°F (10°c to 45°c)
Relative Humidity: 15 to 90 percent (non-condensing)
Altitude: -60m to 3000m (-187 ft to 9840 ft)
Vibration: 0.1G ± 10% 5 to 500 Hz
ESD: No product damage or loss of data with up to a 20KV discharge at any point accessible to the user, except I/O ports.
Thermal Shock: 10 c for 3 hrs., power on, raise temp., 5 c/min. to 45 c for 5 hrs., power off, drop temp. 5 c/min to 10 c. Repeat cycle 5 times, no damage.

4.2 STORAGE ENVIRONMENT

Temperature: (30°c to 60°c)
Relative Humidity: 0 to 90 percent (non-condensing)
Altitude: -60m to 3000m (-198 ft to 9840 ft)
Vibration: 1.5G ± 10%, 5 to 500 Hz
ESD: No product damage with up to a 20KV discharge at any point accessible to the user, except I/O ports.

5.0 ELECTRICAL SPECIFICATIONS

5.1 STATIC PARAMETERS

5.1.1 Power Requirements

Input Voltage: 9.0 Vac (min)
Input Frequency: 60 Hz ± 10 Hz
Input Power: 31VA (max)
Output: 5.0 VDC ± 5% 1.7A (max)
*1.7A Current Draw sum of 5A, 5B, and 5C.

5.1.2 Controller Jack

The following is a list of voltages that will be present at the two controller jack upon initial power-up.

PIN #	VOLTAGE
1	+5VDC(nom) Vcc(max) - 1% (min)
2	+5VDC(nom) Vcc(max) - 1% (min)
3	+5VDC(nom) Vcc(max) - 1% (min)
4	+5VDC(nom) Vcc(max) - 1% (min)
5	OVDC
6	+5VDC(nom) Vcc(max) - 1% (min)
7	+5VDC(nom) Vcc(max) - 1% (min)
8	GND
9	OVDC

5.2 Serial I/O Interface

5.2.1 SIO Static Voltages

The following is a list of voltages that will be present at the 13 pin serial I/O connector upon initial power-up.

PIN #	VOLTAGE
1	5VDC $\pm$ 1%
2	5VDC $\pm$ 1%
3	5VDC $\pm$ 1%
4	OVDC
5	5VDC $\pm$ 1%
6	OVDC
7	5VDC $\pm$ 1%
8	OVDC
9	5VDC $\pm$ 1%
10	5VDC $\pm$ 1%
11	5VDC $\pm$ 1%
12	OVDC
13	5VDC $\pm$ 1%

5.2.2 SIO Electrical Specifications

5.2.2.1 Peripheral Input

VIH = 2.0V (min) Vcc (max)
VIL = 0.0V (min) 0.4V (max)

IIH = 20 A (max) @ VIH = 2.0V
IIL = 5 A (max) @ VIL = 0.4V

5.2.2.2 Peripheral Output (Open Collector)

VOH* = 4.5V (min) Vcc (max)
VOL = 0.4V (max) @ 1.6 mZ

* With 100K external pull-up resistor

5.2.2.3 VCC/READY Input*

VIH = 2.0V (min) @ IIH = 1mA (max)
VIL = 0.4V (max)

* Input goes low when open.

5.2.3 SIO Functional Description

The Atari 1200XL communicates with peripheral devices over a 19.2K baud asynchronous serial port. Data is transmitted and received as 8 bits of serial data (LSB sent first) preceeded by a logic zero start bit and succeeded by a logic one stop bit. The serial data out is transmitted as positive logic. The serial DATA OUT line always assumes its new state when the serial CLOCK OUT line goes high; CLOCK OUT goes low in the center of the DATA OUT time.

The bus protocol specifies that all commands must originate from the computer, and that peripherals will present data on the bus only when commanded to do so. Every bus operation will go to completion before another bus operation is initiated (no overlap). An error detected at any point in the bus operation will abort the entire sequence. A bus operation consists of the following elements:

Command Frame (From Computer)

Acknowledge Frame (From Peripheral)

Optional Data Frame (To or From Computer)

Complete Frame (From Peripheral)

5.2.3.1 Command Frame

The serial bus protocol provides for three types of commands:

1) Data Send
2) Data Receive
3) Immediate (No Data-Command Only)

There is a common element in all three types, a command frame, consisting of five bytes of information sent from the computer while the command line is low. The format of the command frame is as follows:

Device I.D.
Command
Auxilliary #1
Auxilliary #2
Checksum

The Device I.D. specifies which of the serial bus devices is being addressed (see Appendix A for a list of devices I.D.'s).

The command byte contains a device dependant command (see Appendix A for a list of device commands).

The Auxilliary bytes contain more device dependant information.

The checksum byte contains the arithmetic sum of the first four bytes (with cary added back after every addition).

5.2.3.2 Acknowledge Frame

The peripheral being addressed will normally respond to a command frame by sending an ACK byte ($41) to the computer; if there is an error in the command frame, the peripheral will not respond.

5.2.3.3 Data Frame

The data frame may originate at the computer or peripheral depending on the command. The computer and peripherals expect fixed length data frames. The data frame length is fixed function of the device type and command.

The checksum value in the data frame is the arithmetic sum of all data frame bytes preceeding the checksum, with the carry from each addition being added back.

In the case of the computer sending a data frame to a peripheral, the peripheral is to send an ACK ($41) if the data frame is acceptable or a NAK ($4E) if the data frame is nonacceptable.

5.2.3.4 Complete Frame

A peripheral is expected to send an operation complete byte ($43) at the time the command operation is complete. If the operation is cannot go to normal, error-free competition, the peripheral will respond with an error byte ($45) instead of complete.

5.2.4 SIO Timing Diagrams

The following is the timing diagrams for the three types of command sequences; data send, data receive and immediate.

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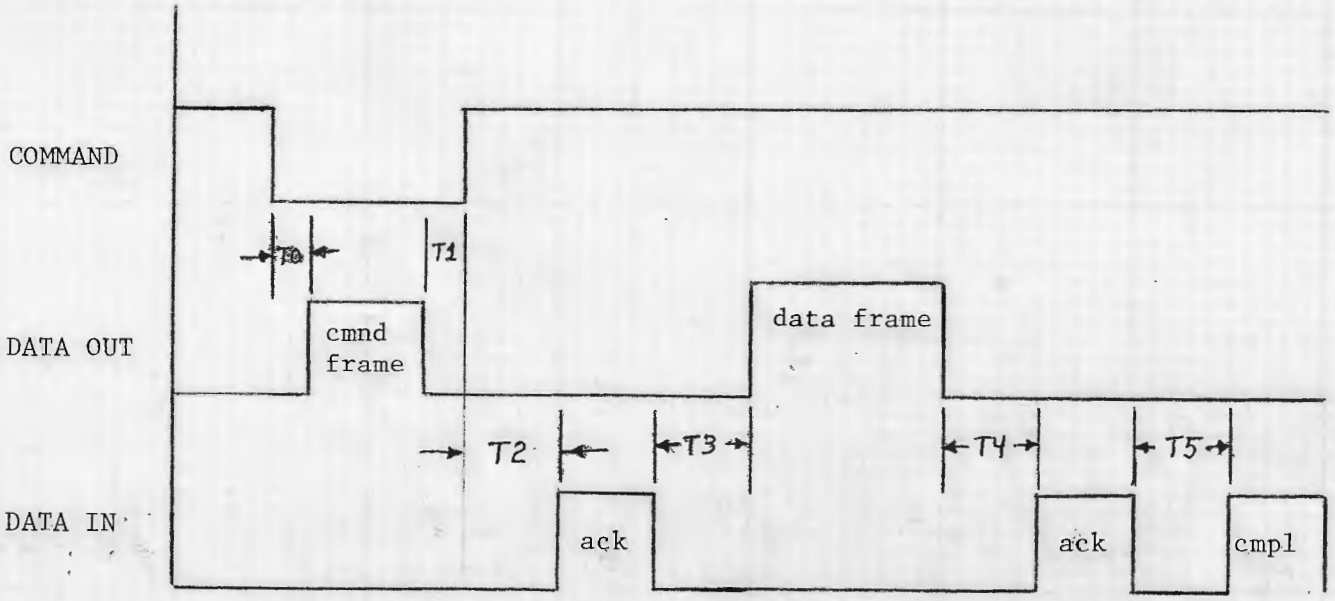

DATA SEND SEQUENCE

T0: = 750µsec (min)
1600µsec (max)

T1: = 650µsec (min)
950µsec (max)

T2: = 0µsec (min)
16msec(max)

T3: = 1000µsec (min)
1800µsec (max)

T4: = 850µsec (min)
16msec (max)

T5; = 250µsec (min)
255 sec (max)

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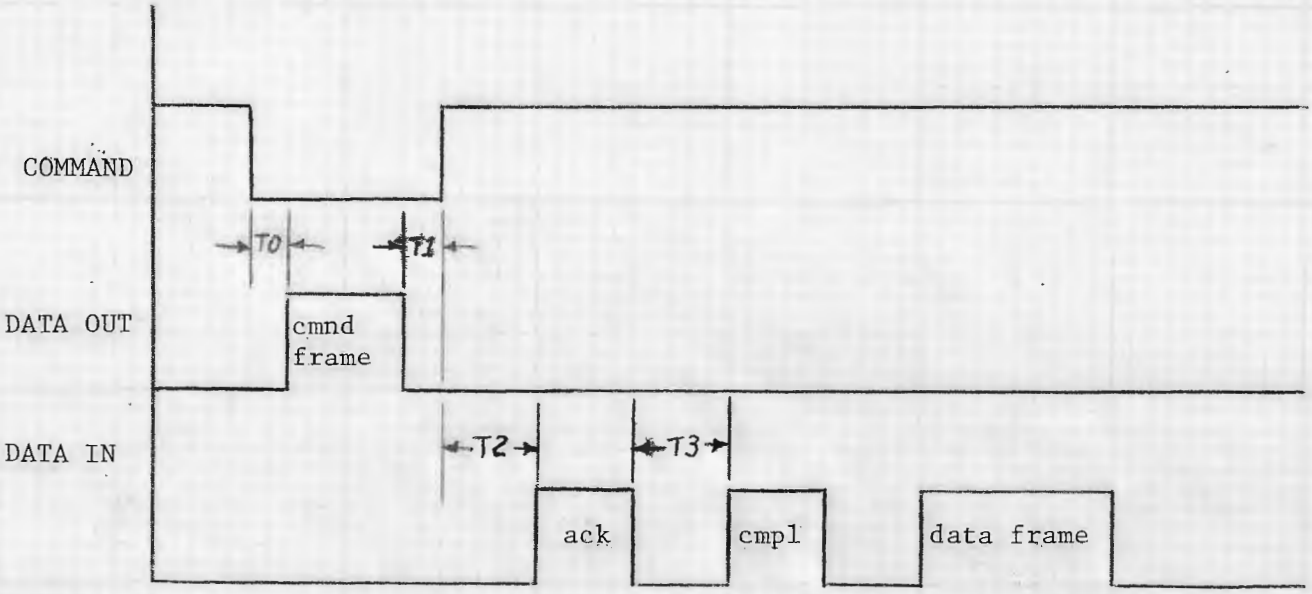


DATA RECEIVE SEQUENCE

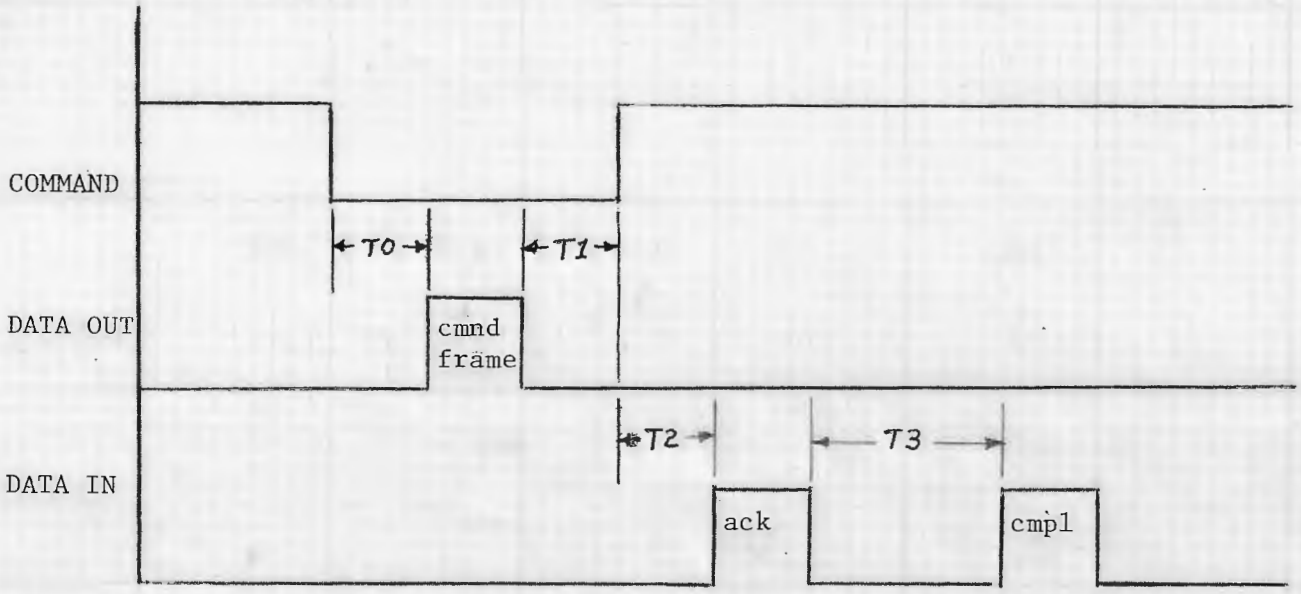
T0: 750 µsec (min)
1600 µsec (max)

T1: 650 µsec (min)
950 µsec (max)

T2: 0 µsec (min)
16 msec (max)

T3: 250 µsec (min)
255 sec (max)

REV	REVISIONS DESCRIPTION	DATE	APPROVED



IMMEDIATE SEQUENCE

T0: 750 µsec (min)
1600 µsec (max)

T1: 650 µsec (min)
950 µsec (max)

T2: 0 µsec (min)
16 msec (max)

T3: 250 µsec (min)
255 µsec (max)

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5.3 The following are timing diagrams and their associated descriptions. These timing diagrams are for the digital section of the Atari 1200XL. All values are to be considered as nominal values.

5.3.1 Clock Timing

The basic oscillator for the Atari 1200 is located at U19 PIN 28. It is asymetrical level signal with a period of 280 ns (3.58 MHZ).

FØ0 is a TTL signal located at either U20 PIN 35 or U19 PIN 29. There is an 80 ns delay between the rising edge of the basic osc. and FØ0. FØ0 has a period 280 ns. The high TTL pulse has a duration of 160 ns. There is a 60 ns delay between the falling edge of the osc. to the falling edge of FØ0.

ANTIC Ø0 is a TTL signal located at U20 PIN 34. ANTIC Ø0 has a period of 560 ns. There is a 180 ns delay between the rising edge of the osc. and the falling edge of ANTIC Ø0. The low TTL pulse of ANTIC Ø0 has a duration of 260 ns. There is a 440 ns delay between the rising edge of the osc. and the rising edge of ANTIC Ø0. The high TTL pulse of ANTIC Ø0 has a duration of 300 ns.

CPU Ø0 is located at U21 PIN 37 and is exactly the same signal as ANTIC Ø0 except that there is a 10 ns delay between CPU Ø0 and ANTIC Ø0. This is caused by the propagation delay of U17.

CPU Ø1 is a TTL signal located at U21 PIN 3 and has a period of 560 ns. There is a 240 ns delay between the rising edge of the OSC and CPU Ø1. The high TTL pulse has a duration of 240 ns. The low TTL pulse has a duration of 320 ns.

CPU Ø2 is asymetrical TTL signal located at U21 PIN 39 and has a period of 560 ns. There is a 210 ns delay between the rising edge of the OSC to the falling edge of CPU Ø2. On all of the following timing diagrams CPU Ø2 will be referred to as the clock.

ANTIC Ø2 is located at U20 PIN 29 and is exactly the same signal as CPU Ø2 except that there is a 10 ns delay between CPU Ø2 and ANTIC Ø2. This is caused by the propagation delay of U17.

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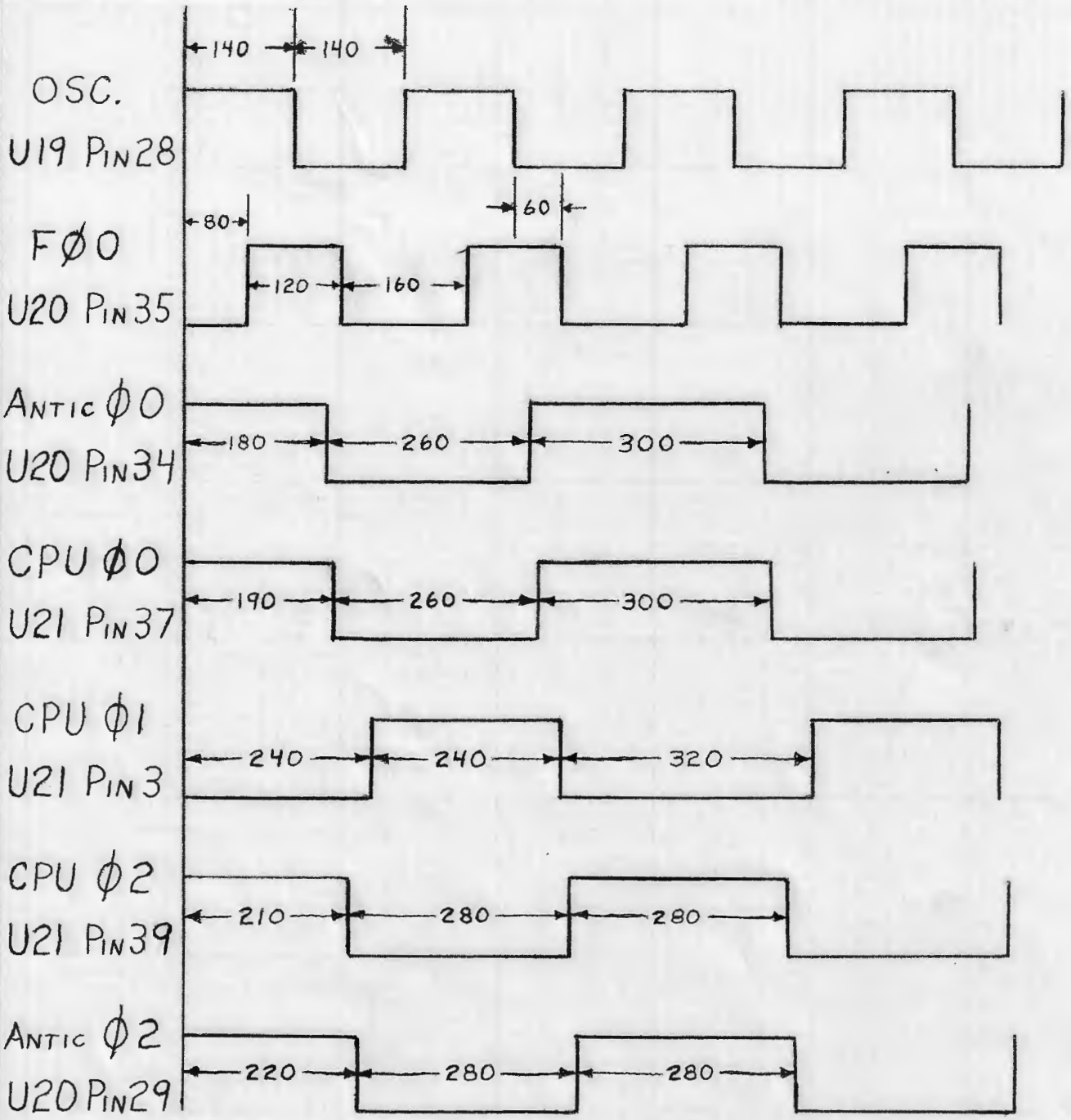

CLOCK TIMING (all MEASUREMENTS IN NANO-SECONDS)

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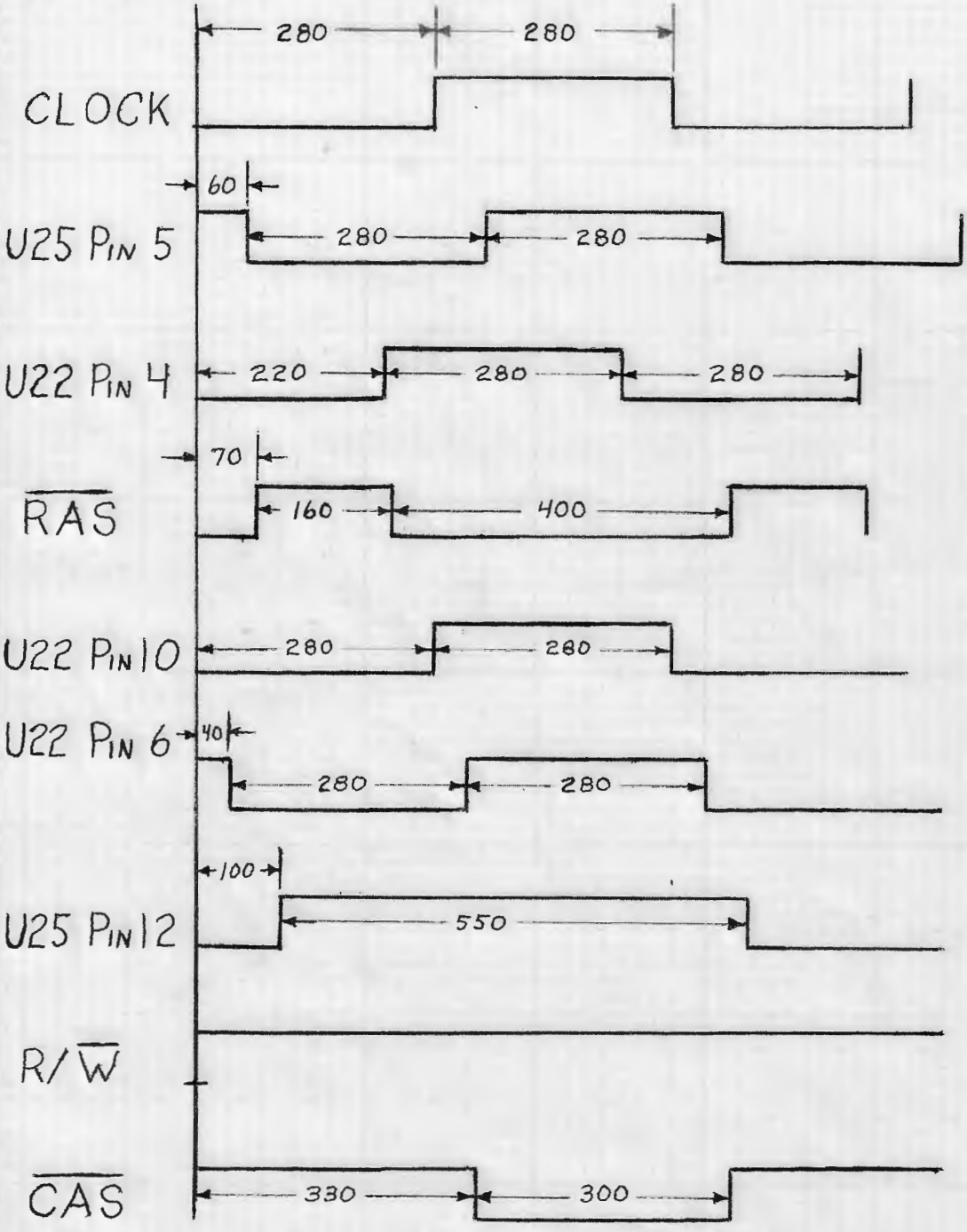
5.3.2 Ram Cycle (Read)

The following is a description of the $\overline{RAS}$ and $\overline{CAS}$ signals as they occur during the RAM cycle read. These signals and their associated timing delays are to be considered nominal values.

U22 PIN 4 delays the clock by 190 ns it is further delayed by the two schmidt triggers (U16) to provide a total delay of 220 ns. At this time at U25 PINS 2 and 3 are high which causes $\overline{RAS}$ to go low. $\overline{RAS}$ will remain low for 400 ns.

U22 PIN 6 delays the clock by 315 ns. It was inverted and delayed by the hex schmitt trigger (U14). At this time at U25 PINS 1, 12, and 13 are high. PIN 12 is $\overline{CI}$ from U14 and PIN 13 is $\overline{WRT}$. With PIN 1, 12, and 13 high $\overline{CAS}$ goes low. $\overline{CAS}$ will remain low for 300 ns.

REV	REVISIONS DESCRIPTION	DATE	APPROVED



RAM CYCLE (READ) ALL MEASUREMENTS IN NANO-SECONDS

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5.3.3 Ram Cycle (Write)

U25 (and-or-invert gate) PIN 5 is a TTL signal. This signal is basically the clock signal delayed 60 ns. 25 ns ± 5% of the delay is caused by U22 (TTL delay line) and the remaining 35 ns is caused by the propagation delay of the two hex schmidt triggers (U16). This causes $\overline{RAS}$ and $\overline{CAS}$ to go high 10 ns later.

U22 PIN 4 delays the clock signal by 220 ns. 190 ns ± 5% of the delay is caused by the delay line the remaining delay is due to the propagation delay of U16. At this time U25 has PIN 2 high, PIN 3 high, PIN 4 high, and PIN 5 low. This causes $\overline{RAS}$ to go low.

U22 PIN 10 delays the clock by 280 ns so that the chip select lines of U7 and U10 (memory multiplexers) are in sync with the clock.

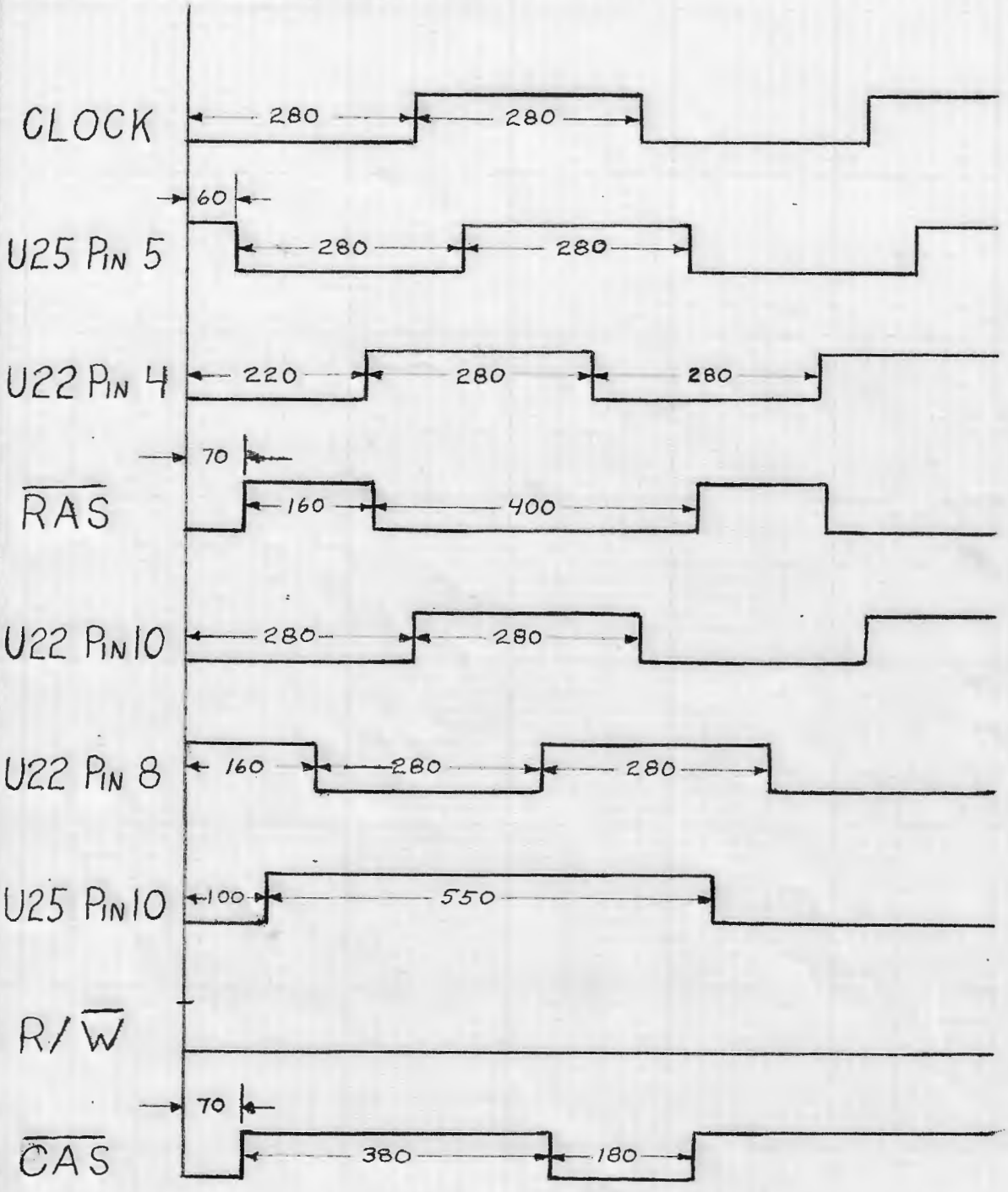
U22 PIN 8 delays the clock by 440 ns ± 10%. The command input from U14 (memory mapper) passes thru U11 (transparrent latch) to U25 PINS 10 and 12.

U25 PIN 10 ($\overline{WR}$) from J4 PIN R (Cartridge) passes thru U11 to U25 PIN 13 and to PIN 3 ($\overline{WRT}$) of U1, U2, U3, U4, U5, U6, U8, and U9 (RAM).

When U22 PIN 8 goes high, U25 PIN 1 is high, PIN 13 is low, PIN 12 is high, PIN 9 is high, PIN 11 is high, and PIN 10 is high. This cause $\overline{CAS}$ to go low 10 ns later. 10 ns after U25 PIN 5 goes low $\overline{RAS}$ and $\overline{CAS}$ go high.

During the RAM write cycle $\overline{RAS}$ has a period of 560 ns, a positive pulse duration of 160 ns and a negative pulse duration of 400 ns. The $\overline{CAS}$ signal also has a period of 560 ns but with a positive pulse duration of 380 ns and a negative pulse duration of 180 ns.

REV	REVISIONS DESCRIPTION	DATE	APPROVED



RAM CYCLE (WRITE) ALL MEASUREMENT IN NANO-SECONDS

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5.3.4 MMU Timing (ROM-Cycle-LB)

The following is a description of the MMU timing signal during the ROM cycle lower byte. The timing for the signals are to be cosidered nominal values.

100 ns after the falling edge of the clock the $\overline{LB}$ (Lower Byte, U14 PIN 13) signal will go low. At the same time $\overline{CI}$ (RAM disable, U14 PIN 16) will also go low.

On the next rising edge of the clock the contents of address lines A11, A12, A13, A14, and A15 will be considered valid if $\overline{REN}$ (ROM enable, U14 PIN 9) is high and $\overline{REF}$ (Refresh, U14 PIN 9) is high. Valid addresses for the lower byte will be from C00D to CFFF or D800 to DFFF or 5000-57FF.

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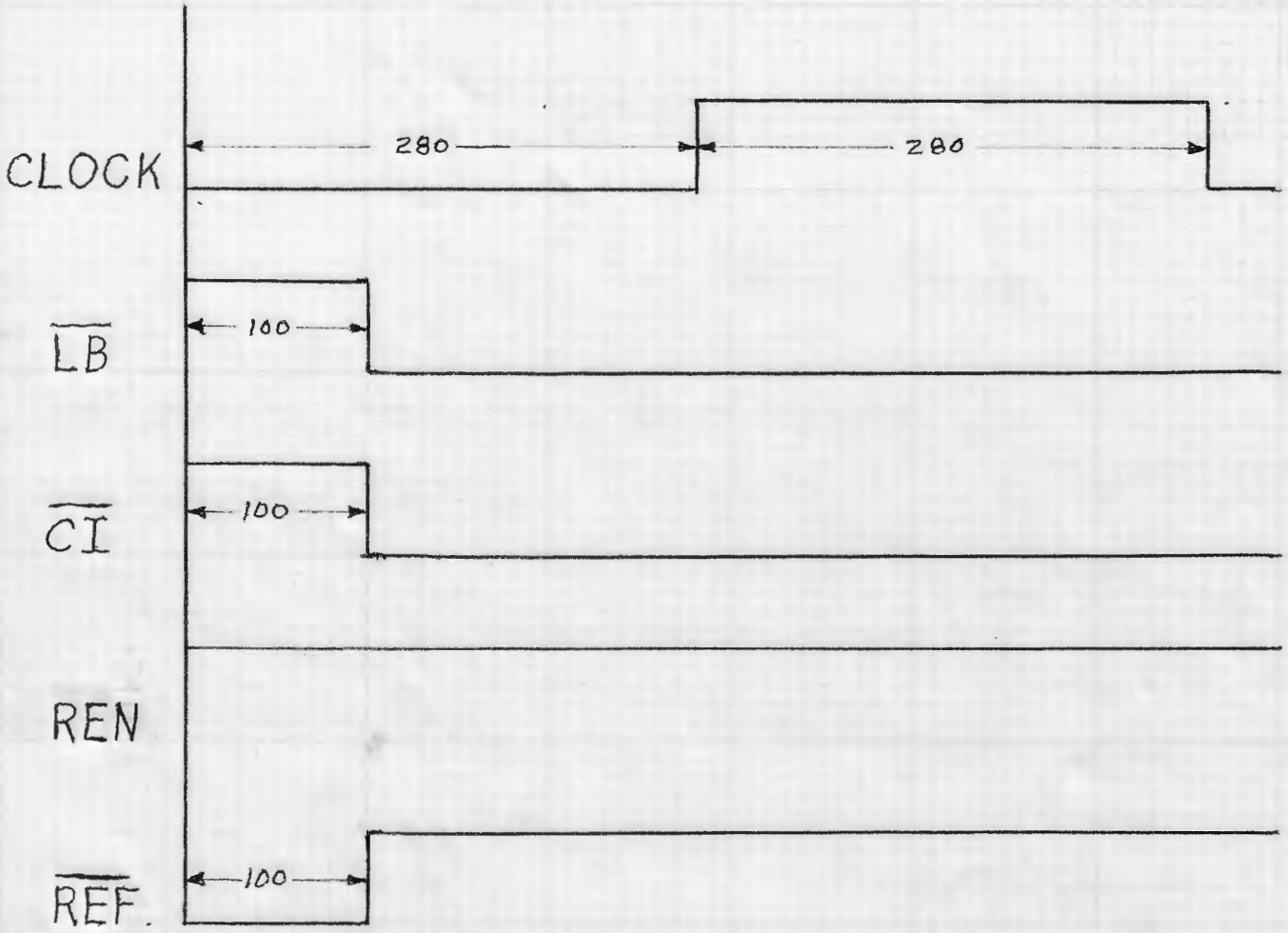

MMU TIMING (ROM CYCLE - LB) ALL MEASUREMENTS IN NANO-SECONDS

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5.3.5 MMU Timing (ROM-Cycle-UB)

The following is a description of the MMU timing signals during the ROM cycle upper byte. The signals are to be considered to be nominal values.

100 ns after the falling edge of the clock the $\overline{UB}$ (Upper Byte, U14 PIN 16) at this time should also go low or already be low. After this time the contents of the address lines (A11, A12, A13, A14 and A15) become valid. Valid addresses for the upper byte must be between E000-EFFF.

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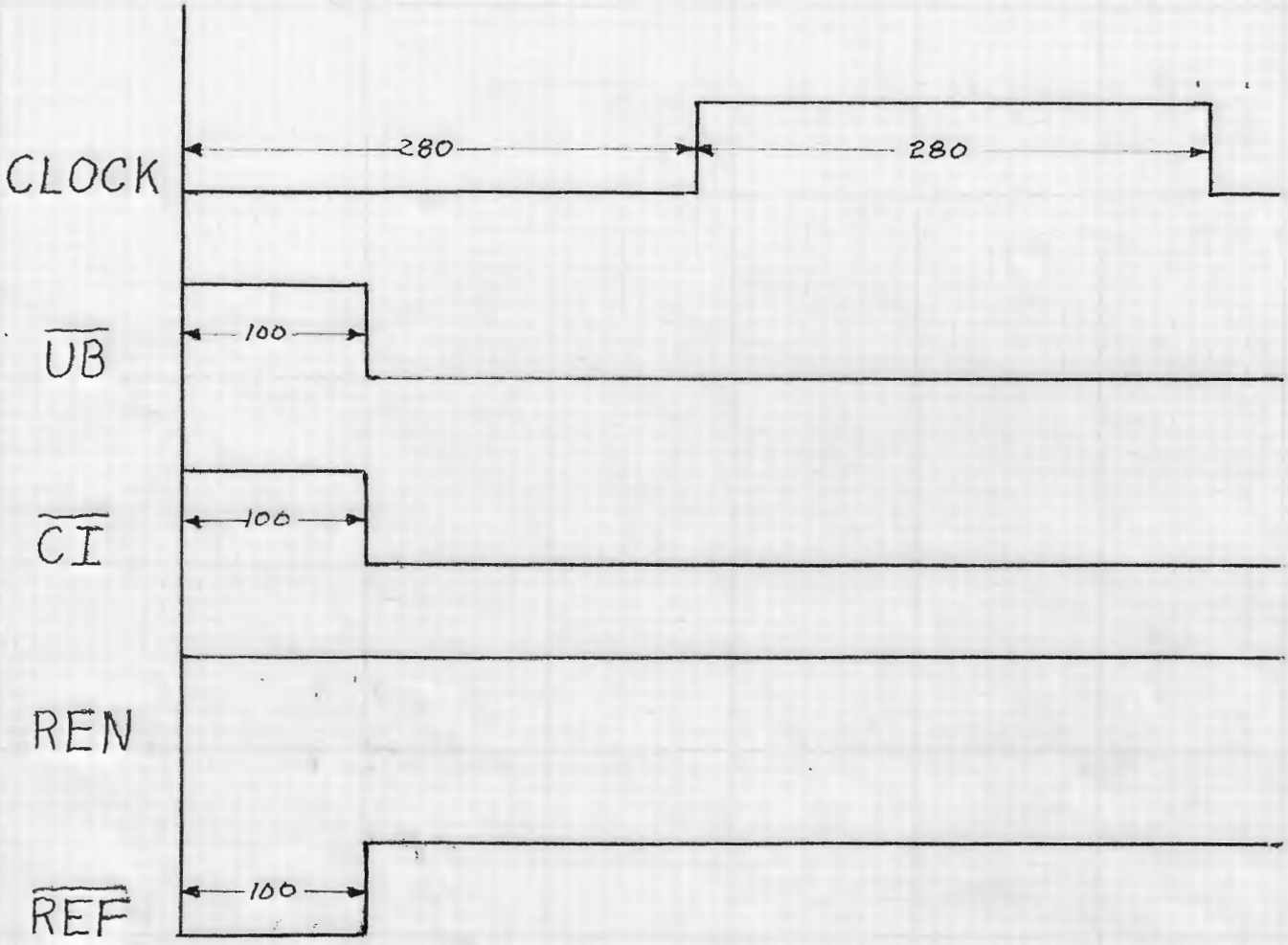

MMU TIMING (ROM CYCLE - UB) ALL MEASUREMENTS IN NANO-SECONDS

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5.3.6 MMU Timing (I/O Cycle)

The following is a description of the MMU timing signals during the I/O cycle. The signals are to be considered to have nominal values.

100 ns after the falling edge of the clock $\overline{IO}$ (Input/Output enable U14 PIN 17) will go low. After this time the contents of the address lines (A11, A12, A13, A14, and A15) will contain a valid I/O address. The valid I/O address will be from D000 to D7FF.

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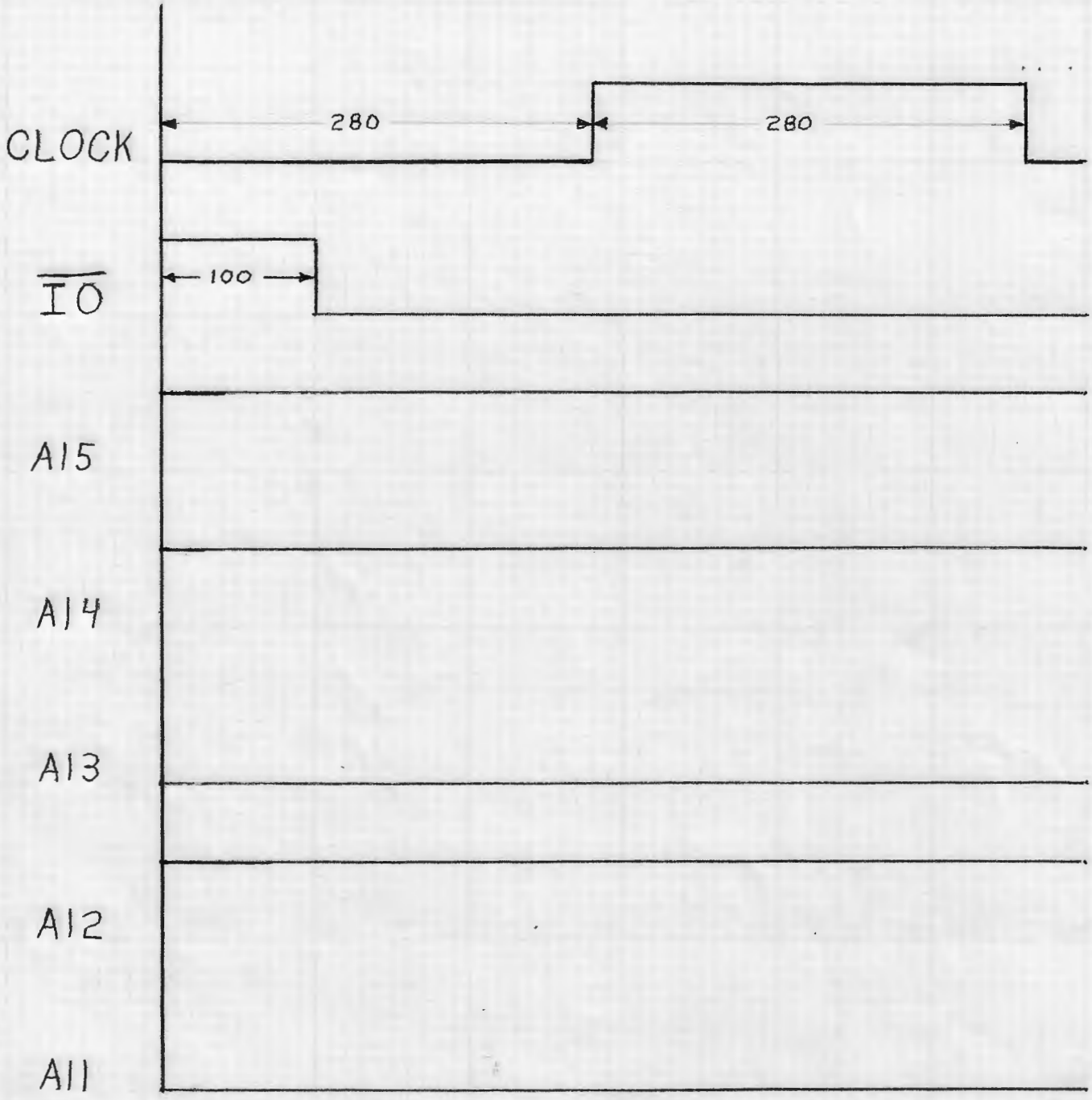

MMU TIMING (I/O CYCLE) ALL MEASUREMENTS IN NANO-SECONDS

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5.3.7 MMU Timing (Cartridge Cycle)

The following is a description of the MMU timing signals for the cartridge cycle. The signals are to be considered to have nominal values.

100 ns after the falling edge of the clock $\overline{S5}$ (Cartridge select-upper byte-U14 PIN 12) will go low. At this time $\overline{IO}$ must be high, $\overline{CI}$ must be low, $\overline{REF}$ must be high and RD5 must be high. With all of these conditions met the contents of the address lines (A11, A12, A13, A14 and A15) will contain a valid cartridge address. Valid upper cartridge address will be from A000 to BFFF.

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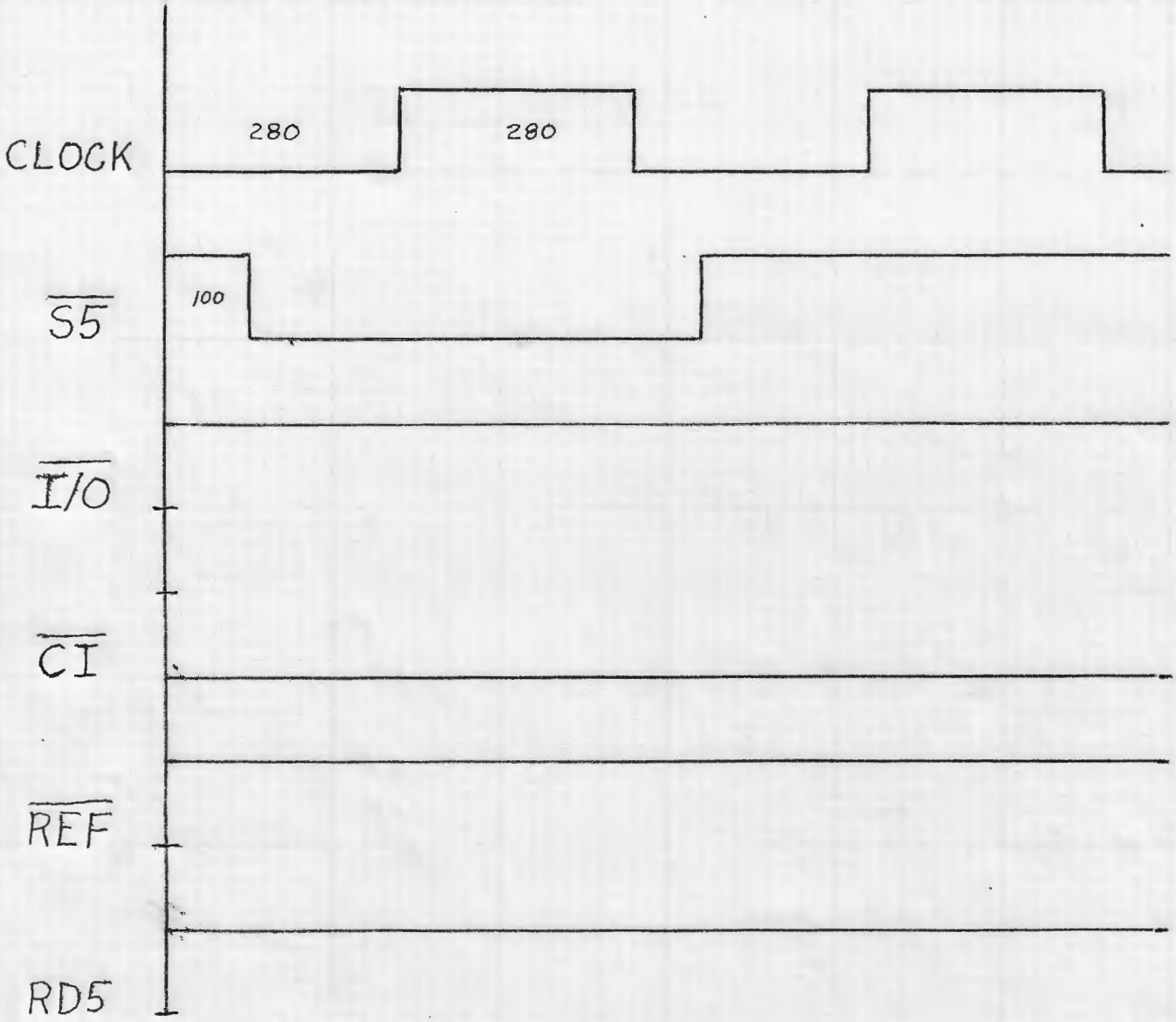

MMU Timing (Cartridge Cycle) all measurements in nano-seconds

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5.3.8 MMU Timing (Refresh Cycle)

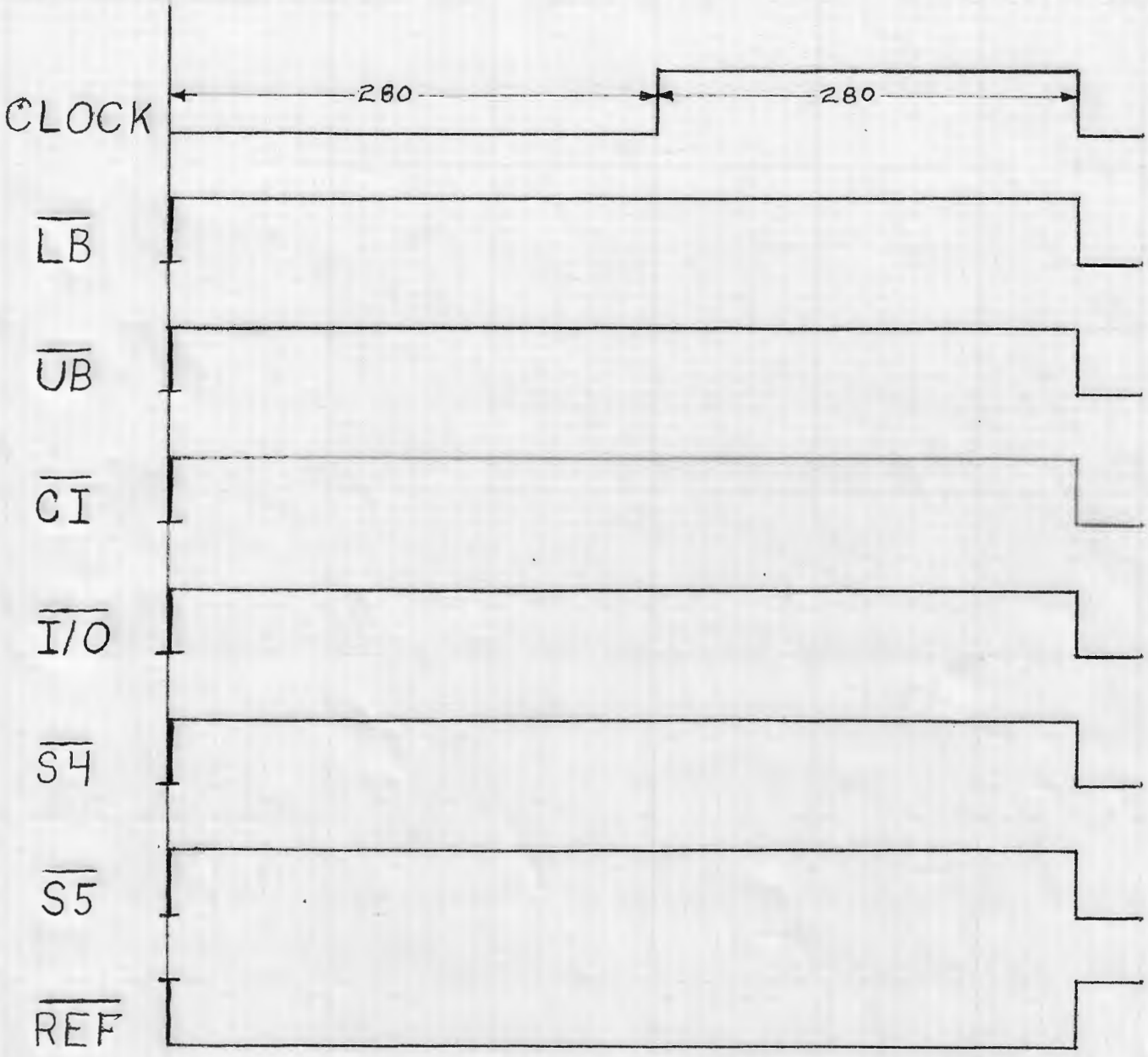
The following is a description of the MMU timing signals during the refresh cycle. The signals are to be considered nominal values.

The following conditions must be met in order for a valid refresh signal to occur:

$\overline{LB}$ (Lower Byte U14 PIN 13) must be high
$\overline{UB}$ (Upper Byte U14 PIN 15) must be high
$\overline{CI}$ (Ram Disable U14 PIN 16) must be high
$\overline{IO}$ (Input/Output U14 PIN 17) must be high
$\overline{S4}$ (Lower Byte Cartridge select U14 PIN 19) must be high
$\overline{S5}$ (High Byte Cartridge select U14 PIN 12) must be high

One clock cycle after ANTIC halts the CPU a refresh signal will occur.

REV	REVISIONS DESCRIPTION	DATE	APPROVED



MMU TIMING (REFRESH CYCLE) ALL MEASUREMENTS IN NANO-SECONDS

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A	C061217	A
SCALE	SHEET 28 OF 41	

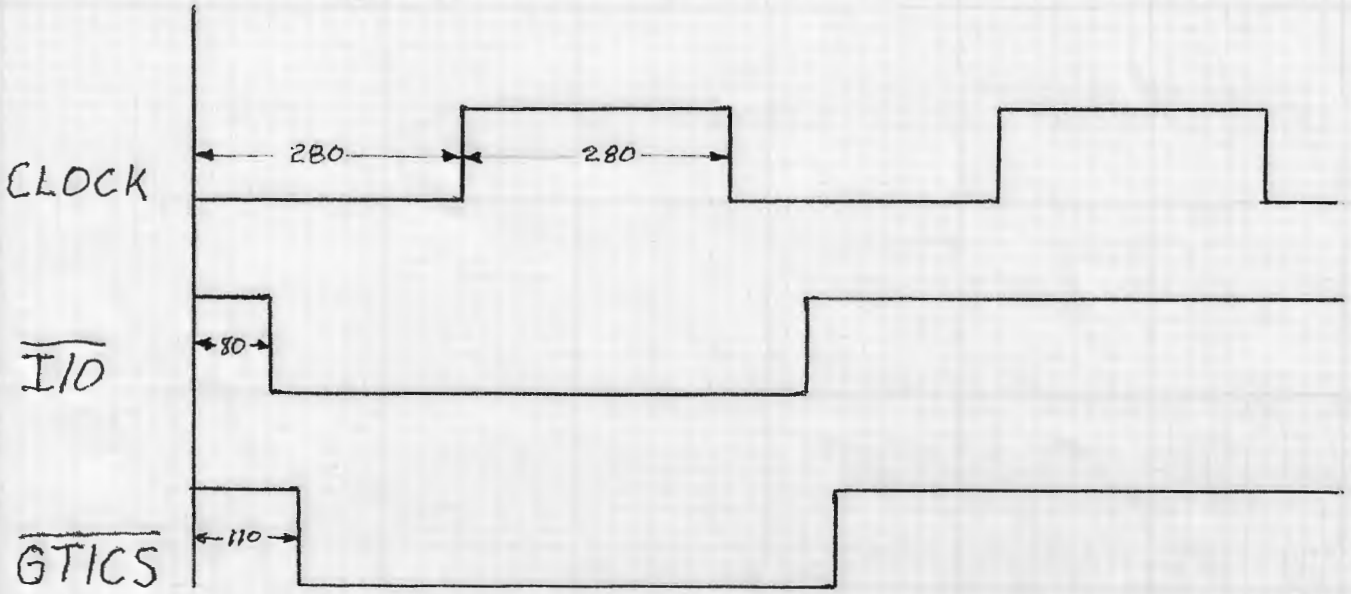
REV	REVISIONS DESCRIPTION	DATE	APPROVED

5.3.9 I/O Decoding (GTIA)

The following is a description of the I/O decoding signals for GTIA. The signals are to be considered to have nominal values.

80 ns after the falling edge of the clock $\overline{IO}$ goes low. 30 ns later $\overline{GTICS}$ (GTIA chip select U19 Pin 32) will go low. At this time the contents of address line A8, A9, and A10 will contain a valid GTIA address. Valid addressed for GTIA will be from D000 to D0FF.

REV	REVISIONS DESCRIPTION	DATE	APPROVED



I/O DECODING (GTIA) ALL MEASUREMENTS IN NANO-SECONDS

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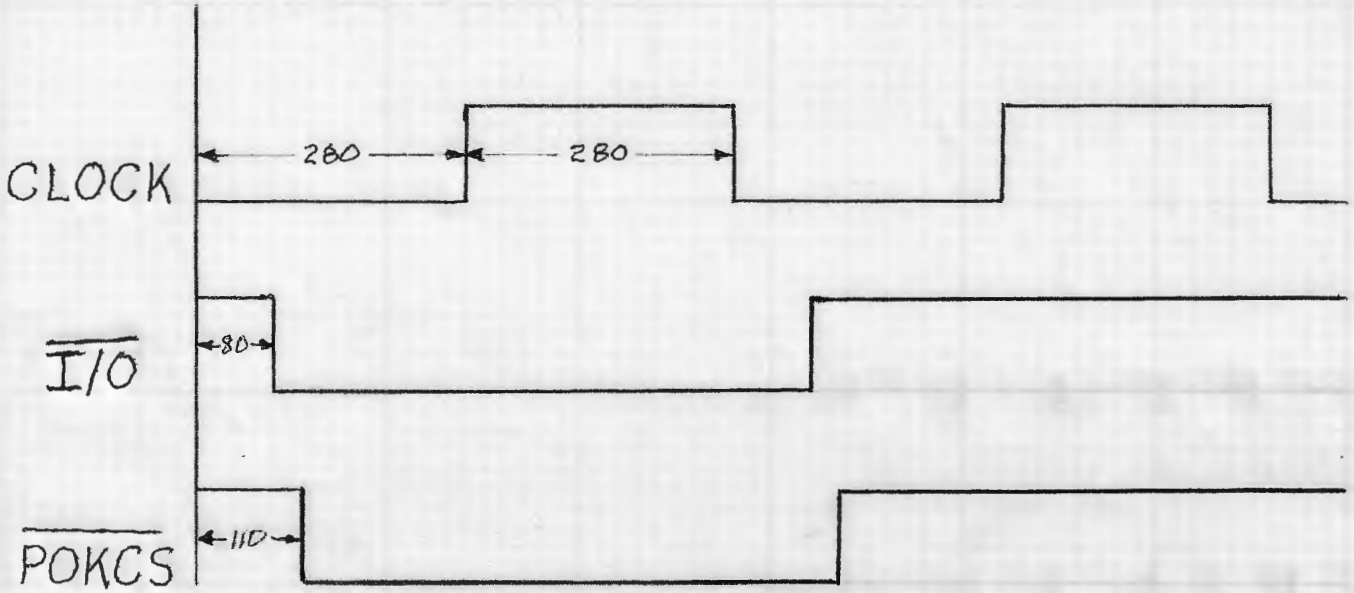
REV	REVISIONS DESCRIPTION	DATE	APPROVED

5.3.10 I/O Decoding (POKEY)

The following is a description of the I/O decoding signal for POKEY. The signals are to be considered to have nominal values.

80 ns after the falling edge of the clock $\overline{IO}$ will go low. 30 ns later $\overline{POKCS}$ (POKEY chip select U24 PIN 30) will go low. At this time the contents of the address lines (A8, A9 and A10) will contain a valid POKEY address. Valid POKEY addresses will be from D200 to D2FF.

REV	REVISIONS DESCRIPTION	DATE	APPROVED



I/O DECODING (POKEY) ALL MEASUREMENTS IN NANO-SECONDS

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	SCALE	SHEET 32 OF 41	

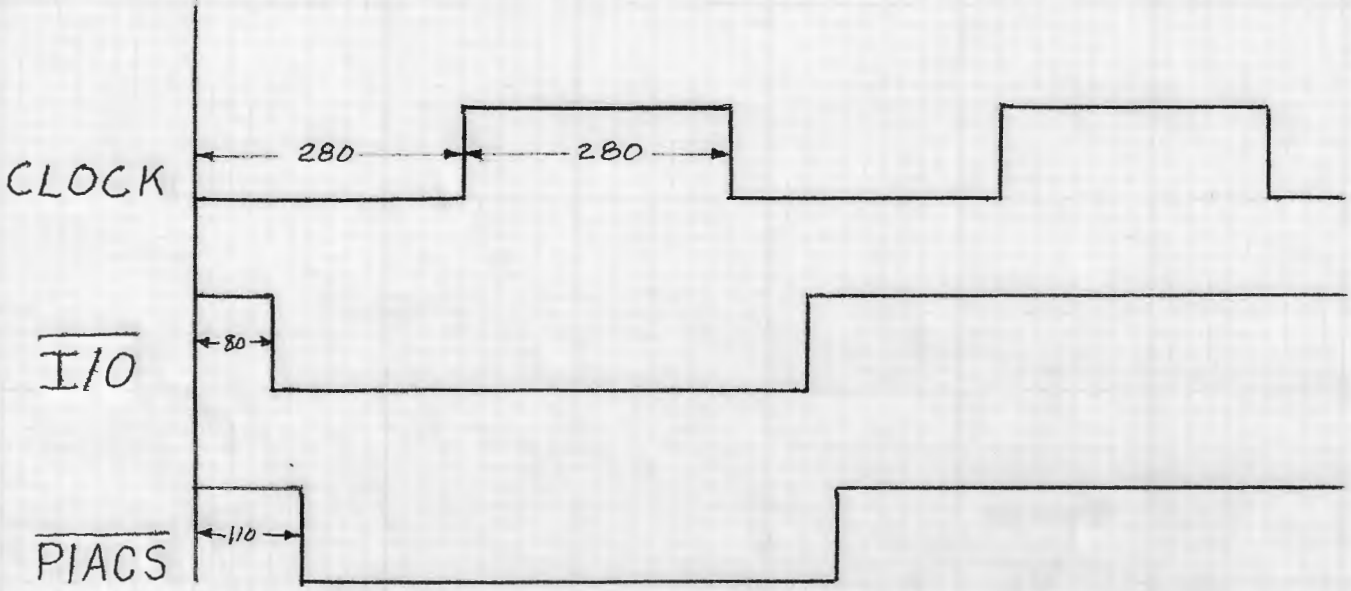
REV	REVISIONS DESCRIPTION	DATE	APPROVED

5.3.11 I/O Decoding (PIA)

The following is a description of the I/O decoding signals for the PIA. The signals are to be considered to have nominal values.

80 ns after the falling edge of the clock $\overline{IO}$ will go low, 30 ns later $\overline{PIACS}$ will go low. At this time the contents of address lines A8, A9 and A10 will contain a valid PIA address. Valid PIA address is from D300 to D3FF.

REV	REVISIONS DESCRIPTION	DATE	APPROVED



I/O DECODING (PIA) ALL MEASUREMENTS IN NANO-SECONDS

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SIZE	DRAWING NO.	REV
A	C061217	A
SCALE	SHEET 34 OF 41	

5.4 VIDEO

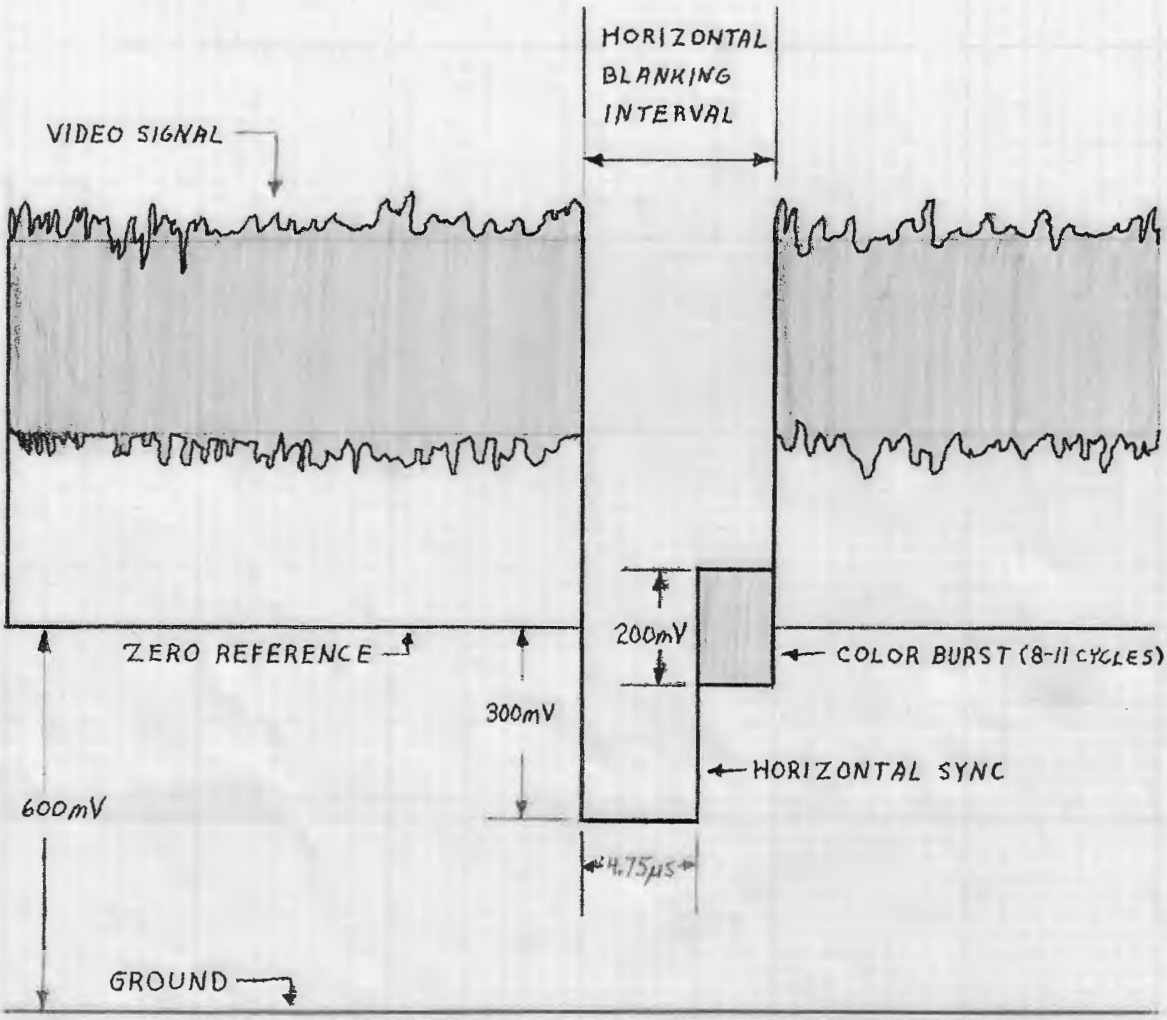
This section describes the video signals necessary for correct function of the video section of the Atari 1200XL. All signals in this section are taken from the common node of R24, R28, R44, and L3. The signal at this point is the composite video signal (chrominance, luminance and sync).

One line of video information contains chromance and luminance (video signal), horizontal blanking interval, horizontal sync, and color burst. The zero reference for the video signal is off set from ground by + 600 mVDC.

The horizontal blanking interval has a pulse width of 10μs $\pm$ 1μs. The horizontal sync pulse and the color burst signal occur during the horizontal blanking interval. Thr horizontal sync pulse is a -300 mV pulse (referenced to video zero reference) with a pulse width of 4.75μs $\pm$ 0.5μs. The color burst is a 200mV Pk-Pk signal consisting of 8-11 cycles at 3.58MHZ (video sub-carrier). The maximum video signal (white screen) has a Pk-Pk value of 900mV above zero reference. The minimum video signal (black screen) is the zero reference. All other chrominance and luminance combinations fall between these two values.

One field of video information contains the vertical blanking interval, vertical sync pulse, and 21 horizontal video lines. The vertical blanking pulse has a pulse width of 1.05ms + 0.25ms. The vertical sync interval is a -300mV pulse (referenced to zero reference) with a pulse width of 200μs $\pm$ 10μs.

REV	REVISIONS DESCRIPTION	DATE	APPROVED



ONE LINE OF COMPOSITE VIDEO

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REV	REVISIONS DESCRIPTION	DATE	APPROVED

5.5 AUDIO

5.5.1 Audio Subcarrier

Frequency: 4.5 MHz + 5KHz
Amplitude: 700mV Pk-Pk
DC Offset: +4.5VDC

5.5.2 Audio Output

Frequency Range:
Amplitude Range: 50mV (Pk-Pk) - 600mV (Pk-Pk)

5.6 TV INTERFACE

5.6.1 Output Voltage

ImV (min) 2mV (max)*

* With 75 OHM Termination.

5.6.2 Channel 2 and 3 Specifications

	BAND	VIDEO CARRIER	AUDIO CARRIER
channel 2	54-60 MHZ	55.25 MHZ	50.75 MHZ
channel 3	60-66 MHZ	61.25 MHZ	65.75 MHZ

5.7 Monitor Interface

5.7.1 Composite Video and Luminance Outputs*

SYNC TIP: 80mV (max)
BLACK LEVEL: 350mV ± 10%.
WHITE LEVEL: 700mV ± 10%.
* with 75 OHM termination.

5.7.2 Audio Output*

Output Voltage: 1v PK-PK (max)
Frequenly Range: 1HZ-49KHZ (3db cutoff)
* with 1.8K OHM Termination

In order to check the following parameters the 1200XL must be hooked up either to a video monitor or a TV set. A basic cartridge must also be inserted in the 1200XL.

5.8.1 Upon system initialization (coldstart) memory location $Ø2DC (732 decimal) will contain ØØ. This can be verified by the following command:

?PEEK(732)

Pressing the help key will change the value at &Ø2DC to $11 (17 decimal).Check this by using the PEEK command shown above.

Pressing the shift and help keys at the same time will change the value at $Ø206 to $51 (81 decimal). Verifty this as in the previous examples:

Pressing the control and help keys at the same time will change the value at $02DC to $91 (145 decimal) verification can be obtained as in previous examples.

5.8.2 Pressing the F1 key will cause the cursor to move up.

5.8.3 Pressing the F2 key will cause the cursor to move down.

5.8.4 Pressing the F3 key will cause the cursor to move left.

5.8.5 Pressing the F4 key will cause the cursor to move right.

5.8.6 Pressing the shift and F1 keys at the same time will cause the cursor to move to the home position.

5.8.7 Pressing the shift and F2 keys at the same time will cause the cursor to move to the lower left corner margin of the screen.

5.8.8 Pressing the shift and F3 keys at the same time will cause the cursor to move to the left margin of the current physical line.

5.8.9 Pressing the shift and F4 keys at the same time will cause the cursor to move to the right margin of the current physical line.

5.8.10 Pressing the control and F1 key once will disable the keyboard and light LED 1. Pressing these keys again will re-enable the keyboard and turn off LED 1.

5.8.11 Pressing the control and F2 will control the RF Modulator/ Switchbox.

5.8.12 Pressing the control and F3 keys once will disable the key click. Pressing them again will re-enable the key click.

5.8.13 Pressing the control and F4 keys once will enable the international character set and turn on LED 2. Pressing them again will re-enable the domestic character set and turn off LED 2.

5.8.14 The controller jack #1 trigger function can be tested with a joystick controller. Plug the joystick into the controller jack #3. Memory location $284 (644 decimal) will have a 1 in it. This can be verified by the following command:

?PEEK(644)

Pressing the trigger button will cause $284 to change to Ø. This is verified by holding the trigger button in while excuting the proceeding command.

5.8.15 The controller jack #2 trigger function can be tested in the same manner as #1 except that the joystick must be inserted in jack #3 and the memeory location change from 644 to 645.

5.8.16 The controller jack #1 joystick up function can be tested by plugging a joystick into Jack #1 and pushing the joystick in the up position while excuting the following command:

?PEEK(632)

This location will contain 14 decimal when pushed in the UP position.

5.8.17 The controller jack #2 joystick UP function can be tested in the same manner except that the joystick must be plugged into jack #2 and the memory location changed to 633.

5.8.18 The controller jack #1 joystick down function can be tested by plugging a joystick into jack #1 and pushing the joystick in the down position while executing the following command:

?PEEK(632)

This location will contain 13 decimal when pushed in the down position.

5.8.19 The controller jack #2 joystick down function can be tested in the same manner except that the joystick must be plugged into jack #2 and the memory location changed to 633.

5.8.20 The controller jack #1 joystick left function can be tested in by plugging a joystick into jack #1 and pushing the joystick in the left position while executing the following command:

?PEEK(632)

This location will contain 11 decimal when the joystick is pushed in the left position.

5.8.21 The controller jack #2 joystick left function can be tested in the same manner except that the joystick must be plugged into jack #2 and the memory location changed to 633.

5.8.22 The controller jack #1 joystick right function can be tested by plugging a joystick into jack #1 and plushing the joystick in the right position while executing the following commmand:

?PEEK(632)

This location will contain 7 decimal when the joystick is pushed in the right position.

5.8.23 The controller jack #2 joystick right function can be tested in the same manner except that the joystick must be plugged into jack #2 and the memory location changed to 633.

5.8.24 The controller jack #1 POT A function can be tested by inserting a paddle controller into jack #1. Turn the paddle fully clockwise and execute the following command:

This location will contain 1 decimal when the paddle controller is turned fully clockwise.

Turn the paddle controller fully counter clockwise and execute the same command. The lcoation now contains 228 decimal.

To test controller jack #1 POT B function repeat the test for POT A but change the memory location to 625.

5.8.25 The controller jack #2 POT A and POT B functions can be checked in the same manner as controller #1 except that the paddle controller must be plugged into jack #2 and the POT A memory location changed to 626 and POT B memory location changed to 627.

5.8.26 The 1200XL will pass all the self tests available. Pressing the help key while the power on Atari Logo is on the screen accesses the self test. These tests check the following components.

1. Memory (RAM, ROM and ANTIC)
2. Audio/Visual (ANTIC, GTIA, and POKEY)
3. Keyboard (POKEY, ANTIC)

5.8.27 The 1200XL will pass all the SALT tests on the SALT cartridge (for more information see Test Procedure Standalone Test).

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APPENDIX A

SERIAL BUS DEVICE I.D.'S

Floppy Disks	D1-D4	$31-34
Printer	P1	$40
RS232-C	P2	$4F

SERIAL BUS COMMAND CODES

READ	$52	('R')	Disk
WRITE	$57	('W')	Printer/Disk
STATUS	$53	('S')	Printer/Disk
PUT (NO CHECK)	$50	('P')	Disk
FORMAT	$21	('!')	Disk
DOWNLOAD	$20		
READAODR	$54		
READ SPIN	$51		Disk
MOTOR ON	$55	('U')	Disk
VERIFY SECTOR	$56	('V')	Disk