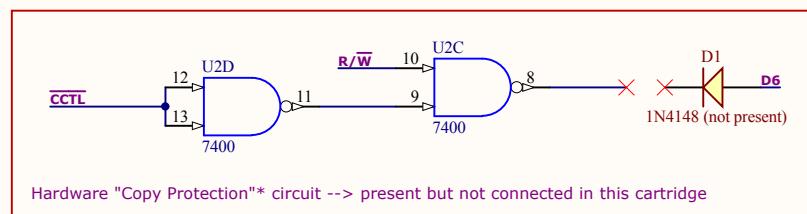
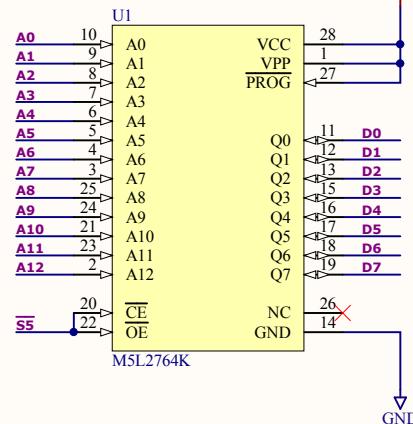
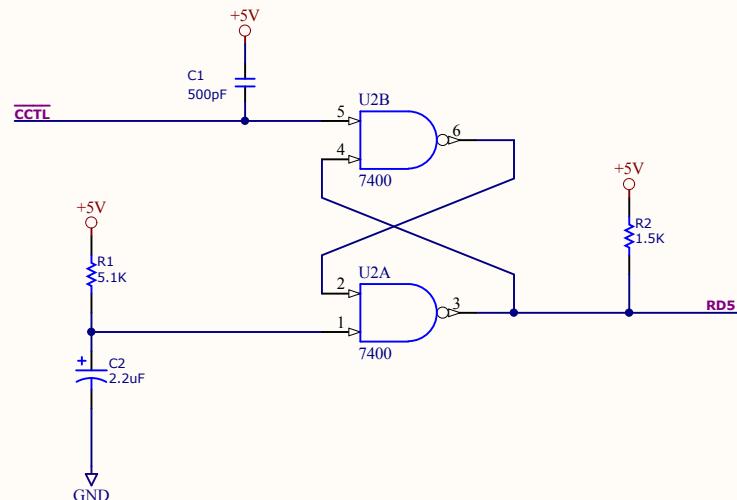


CN1
A0 B5 A0
A1 B4 A1
A2 B3 A2
A3 B2 A3
A4 A3 A4
A5 A4 A5
A6 A5 A6
A7 A6 A7
A8 A7 A8
A9 A8 A9
A10 A13 A10
A11 A12 A11
A12 A9 A12
D0 B10 D0
D1 B9 D1
D2 B8 D2
D3 A10 D3
D4 B6 D4
D5 B7 D5
D6 B11 D6
D7 A11 D7
R/W A14 R/W
PHI2 A15 PH2
CCTL B15 CCTL
RD4 A1 RD5
RD5 B14 RD5
S4 B1 S5
S5 B12 S5
+5V B13 +5V
GND A2 GND
Cart Port



(*) This piece of NAND gates is pulling down the D6 bit of data bus, when any read operation is done at \$D500-\$D5FF area.

Software proceeded by this circuit, reads periodically or in random way the \$D5xx area, then checks that bit D6 is always set to zero, when logic "1" occurs that means that protection circuit doesn't exist.

Title		
Turbo ROM Plus(3) Cartridge		
Size	Number	Revision
A4	(rev. eng. from real hardware)	1.0
Date:	2019-02-09	Sheet 1 of 1
File:	F:\projects\..\TurboROM_plus(3).SchDoc	Drawn By: Seban / Slight